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In re Application of:	Group Art Unit: 2635
MICHAEL L. BEIGEL et al.	Examiner: BRIAN A. ZIMMERMAN
Serial Number: 10/064,380	Telephone: (703) 305-4796
Filing Date: 07/08/02	RECEIVED APR 2 7 2004 Technology Center 2600
For: ELECTRONIC IDENTIFICATION SYSTEM WITH IMPROVED SENSITIVITY	

TRANSMITTAL LETTER - APPEAL BRIEF

Mail Stop Appeal Brief-Patents
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Alexandria, VA 22313-1450

Dear Sir:

Transmitted herewith for filing is the appeal brief in triplicate in support of applicant's appeal to the Board of Patent Appeals and Interferences from the decision of the examiner dated 01/15/04 twice rejecting claims 1-17, 20-25, 32, 36-45, 47-68, and 70-80 of the application referenced above.

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A check for the filing fee in the amount of $165 for a small entity is attached hereto. The Commissioner is hereby authorized to charge any fees under 37 CFR 1.16 and 1.17 which may be required by this paper in excess of the above amount to Deposit Account No. 13-1239. (One additional copy of this Notice is enclosed herewith.)

Respectfully submitted,

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#8

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In re Application of: MICHAEL L. BEIGEL et al. Serial Number: 10/064,380 Filing Date: 07/08/02 For: ELECTRONIC IDENTIFICATION SYSTEM WITH IMPROVED SENSITIVITY	Group Art Unit: 2635 Examiner: BRIAN A. ZIMMERMAN Telephone: 703 305 4796 RECEIVED APR 2 7 2004 Technology Center 2600

APPEAL BRIEF

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INTRODUCTION

The electronic identification system with improved sensitivity, the invention that is the subject of this appeal, relates to cooperative identification systems in which the identifying agency and the object to be identified cooperate in the identification process according to a prearranged scheme. More specifically, the invention relates to systems consisting generically of an interrogator (or "reader") inductively coupled to a transponder (or "tag") where the reader is associated with the identifying agency and the tag is associated with the object to be identified.

The subject invention provides two-way communication between a reader and a tag by means of inductively-coupled coils. The reader drives its coil through capacitors at a driving frequency and the tag detects the reader's signal by means of the tag's inductively-coupled coil connected in parallel with a capacitor. In order to obtain good communication sensitivity, the coil and capacitor in both reader and tag are maintained at or near a state of resonance while communications are taking place by adjusting either intermittently or continually the frequency of the coil driving signal, the inductance of the coil, or the capacitance of the capacitor in the reader and the inductance of the coil or the capacitance of the capacitor in the tag. It may be desirable in certain situations, in order to realize the best communication performance, to maintain the coil and capacitor near resonance but not in a state of resonance.

REAL PARTY IN INTEREST

The real party in interest is: AVID IDENTIFICATION SYSTEMS, INC.
3179 Hamner Avenue, Suite 5
Norco, CA 91760

RELATED APPEALS AND INTERFERENCES

The parent application 08/262,157 (now Pat. No. 6,472,975) was the subject of Appeal No. 1997-2816 before the BPAI and Appeal No. 00-1442 before the Court of Appeals of the Federal Circuit

STATUS OF CLAIMS

Claims 1-80 are pending in the application.

No claims are allowed.

*Claims 18-19, 26-31, 33-35, 46, and 69 are objected to.

**Claims 1-17, 20-25, 32, 36-45,47-68, and 70-80 are rejected and all are subject to appeal.

*Claims objected to are all claims not rejected.

**Rejected claims are all those listed in Sections 1-8 of the 01/15/04 Office Action together with claim 49 which appellants believe the examiner intended to reject as one of the group 48-50.

STATUS OF AMENDMENTS

No amendments were filed subsequent to most recent rejection of the claims by the examiner.

SUMMARY OF INVENTION

1. A reader for use with a tag that communicates data to the reader, the reader comprising:

a transformer having a plurality of windings, each winding having first and second terminals (Specification: ¶¶ 30, 45-47);

a coil driver having first and second output terminals (Specification: ¶ 30);

two capacitors, each capacitor having first and second terminals, the first and second output terminals of the coil driver being connected to the first terminals of the capacitors, the second terminals of the capacitors being connected to the first and second terminals of a winding of the transformer (Specification: ¶ 30);

a coil having first and second terminals connected respectively to the first and second end terminals of a winding of the transformer (Specification: ¶ 30);

a data extractor for extracting data from the signal induced in the coil, the data extractor having first and second terminals connected respectively to first and second terminals of a winding of the transformer (Specification: ¶¶ 30, 36).

2. The reader of claim 1 wherein the transformer has a first winding and a second winding, the capacitors being connected to the first winding, the coil being connected to the second winding, and the data extractor being connected to the first winding (Specification: ¶ 46).

3. The reader of claim 1 wherein the transformer has a first winding and a second winding, the capacitors being connected to the first winding, the coil being connected to the second winding, and the data extractor being connected to the second winding (Specification: ¶ 46).

4. The reader of claim 1 wherein the transformer has a first winding, a second winding,

and a third winding, the capacitors being connected to the first winding, the coil being connected to the second winding, and the data extractor being connected to the third winding (Specification: ¶ 47).

5. A reader for use with a tag, the reader comprising:

a coil (Specification: ¶ 30);

at least one capacitor (Specification: ¶ 30);

a means for coupling the capacitor(s) to the coil (Specification: ¶ 30);

a means for driving the coil through the capacitor(s) with a driving signal (Specification: ¶ 30);

a means for generating the driving signal (Specification: ¶¶ 30, 68-71);

a means for embedding a bit-timing clock signal in the driving signal (Specification: ¶ 82);

a means for embedding a sequence of bits to be communicated to a tag in the driving signal (Specification: ¶ 82).

6. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal to have a first phase when a "0" bit is being transmitted and to have a second phase when a "1" bit is being transmitted (Specification: ¶ 72).

7. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted (Specification: ¶¶ 71-74).

8. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal having a

first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted (Specification: ¶¶ 71-74).

9. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted (Specification: ¶¶ 71-74).

10. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal to have a first frequency when a "0" bit is being transmitted and to have a second frequency when a "1" bit is being transmitted (Specification: ¶¶ 71-74).

11. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted (Specification: ¶¶ 71-74).

12. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted (Specification: ¶¶ 71-74).

13. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted (Specification: ¶¶ 71-74).

14. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal (1) to have a first phase and a first frequency when a "00" bit pair is being transmitted, (2) to have a first phase and a second frequency when a "01" bit pair is being transmitted, (3) to have a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) to have a second phase and a second frequency when a "11" bit pair is being transmitted (Specification: ¶¶ 71-74).

15. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted (Specification: ¶¶ 71-74).

16. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted (Specification: ¶¶ 71-74).

17. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first

frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted (Specification: ¶¶ 71-74).

18. The reader of claim 5 wherein the bit-timing clock signal is used by the tag to control the start time of each bit transmitted to the reader, the reader further comprising:

a means for extracting data communicated by the tag from a coupling-means signal (Specification: ¶¶ 56-62).

19. The reader of claim 18 wherein the tag transmits a first signal during a bit period when a "0" bit is to be communicated and a second signal during a bit period when a "1" is to be communicated, the data-extracting means comprising:

a means for identifying the bit communicated by the tag during each bit period, the start of each bit period being determined by the bit-timing clock signal (Specification: ¶¶ 56-62).

20. The reader of claim of 19 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the coupling-means signal (Specification: ¶¶ 58-59);

a means for translating the weighted integration(s) into a bit value (Specification: ¶ 60).

21. The reader of claim of 19 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the amplitude of the coupling-means signal (Specification: ¶¶ 58-59);

a means for translating the weighted integration(s) into a bit value (Specification: ¶ 60).

22. The reader of claim of 19 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the phase of the coupling-means signal (Specification: ¶¶ 56, 140);

a means for translating the weighted integration(s) into a bit value (Specification: ¶¶ 60).

23. The reader of claim 19 wherein the first signal is a periodic signal with a first value for a predetermined signal parameter and the second signal is the periodic signal with a second value for the predetermined signal parameter, the predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the periodic signal, the bit-identifying means comprising:

a means for generating a first replica of the periodic signal with the first value for the predetermined signal parameter and a second replica of the periodic signal with the second value for the predetermined signal parameter (Specification: ¶ 59);

a means for multiplying the coupling-means signal by the first replica thereby obtaining a first product waveform and by the second replica thereby obtaining a second product waveform (Specification: ¶ 59);

a means for integrating the first and second product waveforms for a bit period and translating the integration results into a bit value (Specification: ¶¶ 59-60).

24. The reader of claim 19 wherein the first signal is a periodic signal with a first value for a first predetermined signal parameter and the second signal is the periodic signal with a second value for the first predetermined signal parameter, the first predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the periodic signal, the periodic signal modulating a second predetermined signal parameter of a carrier signal, the second predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the carrier signal, the bit-identifying means comprising:

a means for demodulating the second predetermined signal parameter of the coupling-means

signal (Specification: ¶¶ 49,140);

a means for generating a first replica of the periodic signal with the first value for the first predetermined signal parameter and a second replica of the periodic signal with the second value for the first predetermined signal parameter (Specification: ¶¶ 59, 140);

a means for multiplying the demodulated coupling-means signal by the first replica thereby obtaining a first product waveform and by the second replica thereby obtaining a second product waveform (Specification: ¶¶ 59, 140);

a means for integrating the first and second product waveforms for a bit period and translating the integration results into a bit value (Specification: ¶¶ 59-60, 140).

25. A reader for use with a tag that transmits a periodic signal having a first frequency when a "0" bit is to be communicated and a second frequency when a "1" bit is to be communicated, the reader comprising:

a means for receiving the tag signal (Specification: ¶¶ 36);

a means for measuring the period of each cycle of the signal received from the tag during a bit period (Specification: ¶¶ 49, 62, 129-130).

26. The reader of claim 25 further comprising:

a means for identifying the bit transmitted by the tag from the measurements of the period of each cycle of the signal received from the tag during a bit period (Specification: ¶¶ 131-135).

27. The reader of claim 26 wherein the means for identifying the bit transmitted by the tag comprises:

a means for identifying the frequency of each cycle of the received signal, the frequency of a cycle being the first frequency if the absolute value of the difference between the period of the

cycle and the period of the first-frequency signal is less than a first predetermined value, the frequency of a cycle being the second frequency if the absolute value of the difference between the period of the cycle and the period of the second-frequency signal is less than a second predetermined value (Specification: ¶¶ 129-135);

a means for identifying the bit transmitted during a bit period from the frequencies of the cycles of the received signal, the bit being a "0" if the number of first-frequency cycles exceeds the number of second-frequency cycles in the bit period, the bit otherwise being a "1" (Specification: ¶¶ 136-138).

28. The reader of claim 26 wherein the means for identifying the bit transmitted by the tag comprises:

a means for identifying the frequency of each cycle of the received signal, the frequency of a cycle being the first frequency if the period of the cycle is greater than a first predetermined value and less than a second predetermined value, the frequency of a cycle being the second frequency if the period of the cycle is greater than a third predetermined value and less than a fourth predetermined value (Specification: ¶¶ 129-135);

a means for identifying the bit transmitted during a bit period from the frequencies of the cycles of the received signal, the bit being a "0" if the number of first-frequency cycles exceeds the number of second-frequency cycles in the bit period, the bit otherwise being a "1" (Specification: ¶¶ 136-138).

29. The reader of claim 25 further comprising:

a means for identifying the beginning of a bit period, the beginning of a bit period being identified by a change greater than a predetermined value in the period of a cycle from one cycle to

the next cycle (Specification: ¶ 136).

30. The reader of claim 25 further comprising:

a means for identifying the frequency of each cycle of the received signal, the frequency of a cycle being the first frequency if the absolute value of the difference between the period of the cycle and the period of the first-frequency signal is less than a first predetermined value, the frequency of a cycle being the second frequency if the absolute value of the difference between the period of the cycle and the period of the second-frequency signal is less than a second predetermined value (Specification: ¶¶ 129-135);

a means for identifying the beginning of a bit period, the beginning of a bit period being identified by a change in frequency from one cycle to the next (Specification: ¶ 136).

31. The reader of claim 25 further comprising:

a means for identifying the frequency of each cycle of the received signal, the frequency of a cycle being the first frequency if the period of the cycle is greater than a first predetermined value and less than a second predetermined value, the frequency of a cycle being the second frequency if the period of the cycle is greater than a third predetermined value and less than a fourth predetermined value (Specification: ¶¶ 129-135);

a means for identifying the beginning of a bit period, the beginning of a bit period being identified by a change in frequency from one cycle to the next (Specification: ¶ 136).

32. A reader for use with a tag that transmits a data sequence to the reader by repeating a message a plurality of times, the message comprising a preamble, a tag data group of T bits, and an error-detecting group of E bits, the preamble consisting of a sync sequence of S bits, the tag data group and the error-detecting group possibly including false-sync sequences, the reader comprising:

a means for receiving the data sequence transmitted by the tag (Specification: ¶¶ 56-62);

a means for detecting each sync sequence in the received data sequence (Specification: ¶¶ 83-93);

a means for identifying the preamble (Specification: ¶¶ 83-93);

a means for extracting the tag data group from the received data sequence utilizing the identification of the preamble (Specification: ¶¶ 87, 91).

33. The reader of claim 32 wherein the preamble identifying means comprises:

a means for detecting errors in the T + E bits following each detected sync sequence assuming that the sequence in question is the preamble, the presence of errors indicating that the sync sequence in question is a false-sync sequence, the absence of errors indicating that the sequence is, in fact, the preamble (Specification: ¶¶ 83-93).

34. The reader of claim 33 wherein the sync sequence detecting means comprises:

a memory for storing (S+T+E) received data bits (Specification: ¶ 86);

a means for determining whether the oldest S bits in memory is a sync sequence (Specification: ¶ 87);

a means for replacing the oldest bit in memory with the next received bit after the memory has been filled with received bits (Specification: ¶ 88);

a control means for causing the determining means and the replacing means to operate alternately after the memory is filled with received bits (Specification: ¶ 88).

35. The reader of claim 33 wherein the sync sequence detecting means comprises:

a memory for storing (S+T+E) received data bits (Specification: ¶ 86);

a first means for determining whether the newest S bits in memory is a sync sequence

(Specification: ¶ 87);

a second means for determining whether the oldest S bits in memory is a sync sequence (Specification: ¶ 87);

a means for replacing the oldest bit in memory with the next received bit after the memory has been filled with received bits (Specification: ¶ 88);

a control means for causing the first determining means and the replacing means to operate alternately until a sync sequence is detected, the control means causing the second determining means and the replacing means to operate alternately if a detected sync sequence is determined to be a false-sync sequence (Specification: ¶ 88).

36. A reader for use with a tag, the reader comprising:

a coil (Specification: ¶ 30);

at least one capacitor (Specification: ¶ 30);

a means for coupling the capacitor(s) to the coil (Specification: ¶ 30);

a means for driving the coil through the capacitor(s) with a driving signal, the means consisting of four field-effect transistors connected in a bridge arrangement, two opposing junctions being connected to a power supply, the driving signal being available at the remaining two opposing junctions, the current flow through the transistors being controlled by a control signal applied to the gate of each transistor (Specification: ¶¶ 30, 68, 75-78);

a means for generating at least one control signal (Specification: ¶¶ 30, 68-69).

37. The reader of claim 36 wherein the bridge circuit comprises two series-connected P- and N-channel field effect transistors connected in parallel, the junction of the P devices and the junction of the N devices being connected to a voltage supply, the driving signal being available at

the junctions of the P and N devices (Specification: ¶¶ 75-78).

38. The reader of claim 37 further comprising:

a diode connected between gate and source of each transistor to protect the gates from voltage spikes (Specification: ¶ 80);

a resistor in series with each gate of each transistor to suppress ringing in the gate circuit when the transistor is turned on (Specification: ¶ 80).

39. The reader of claim 36 wherein the bridge circuit comprises four N-channel field effect transistors connected source to drain, source to source, drain to source, and drain to drain, the junction of the drains and the junction of the sources being connected to a voltage supply, the driving signal being available at the source-drain junctions (Specification: ¶¶ 75-78).

40. The reader of claim 39 further comprising a two-winding transformer associated with each transistor, a control signal being fed into one winding of a transformer, the other winding being connected between gate and source electrodes of the associated transistor (Specification: ¶¶ 30, 68, 75-78).

41. A tag for use with a reader, the tag comprising:

a transformer having a plurality of windings, each winding having first and second terminals (Specification: ¶¶ 39, 96-99);

a coil having first and second terminals connected respectively to the first and second terminals of a winding of the transformer (Specification: ¶¶ 39, 96-99);

a capacitor having first and second terminals connected respectively to the first and second terminals of a winding of the transformer (Specification: ¶¶ 39, 96-99);

a coil driver having first and second terminals connected respectively to the first and second

terminals of a winding of the transformer(Specification: ¶¶ 39, 96-99);

a data extractor for extracting the data from the signal induced in the coil, the data extractor having first and second terminals connected to the first and second terminals of a winding of the transformer (Specification: ¶¶ 101, 96-99);

a power extractor for extracting power from the signal induced in the coil to operate the tag, the power extractor having first and second terminals connected respectively to the first and second terminals of a winding of the transformer (Specification: ¶¶ 43, 96-99).

42. The tag of claim 41 wherein the transformer has a first winding and a second winding, the capacitor, the coil driver, the data extractor, and the power extractor being connected to the first winding, the coil being connected to the second winding (Specification: ¶ 96).

43. The tag of claim 41 wherein the transformer has a first winding and a second winding, the capacitor and the coil driver being connected to the first winding, the coil, the data extractor, and the power extractor being connected to the second winding (Specification: ¶ 96).

44. The tag of claim 41 wherein the transformer has a first winding, a second winding, and a third winding, the capacitor and the coil driver being connected to the first winding, the data extractor and the power extractor being connected to the second winding, and the coil being connected to the third winding (Specification: ¶ 97).

45. The tag of claim 41 wherein the transformer has a first winding, a second winding, a third winding, and a fourth winding, the capacitor and the coil driver being connected to the first winding, the data extractor being connected to the second winding, the power extractor being connected to the third winding, and the coil being connected to the fourth winding (Specification: ¶ 98).

46. The tag of claim 41 wherein the transformer has a first winding, a second winding, a third winding, a fourth winding, and a fifth winding, the capacitor being connected to the first winding, the coil driver being connected to the second winding, the data extractor being connected to the third winding, the power extractor being connected to the fourth winding, and the coil being connected to the fifth winding (Specification: ¶ 99).

47. A tag for use with a reader, the reader communicating a sequence of bits to the tag by transmitting a first signal during a bit period when a "0" bit is to be communicated and a second signal during a bit period when a "1" is to be communicated, the reader embedding a bit-timing clock signal in the transmitted signals, the tag comprising:

a coil (Specification: ¶ 39);

a capacitor (Specification: ¶ 39);

a means for coupling the capacitor to the coil and coupling the coil to at least one other means, the signal(s) provided to the other means as a result of the coupling being called coupling-means signal(s), the combination of the coil, the capacitor, and the coupling means being called the resonating circuit (Specification: ¶ 39);

a means for generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded in the transmitted signals (Specification: ¶¶ 111-118);

a means for identifying the bit being transmitted during each bit period, the beginning and ending of each bit period being indicated by the bit-timing clock signal (Specification: ¶ 122).

48. The tag of claim of 47 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the coupling-means signal (Specification: ¶¶ 122, 58-59);

a means for translating the weighted integration(s) into a bit value (Specification: ¶¶ 122, 60).

49. The tag of claim of 47 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the amplitude of the coupling-means signal (Specification: ¶¶ 122, 58-59);

a means for translating the weighted integration(s) into a bit value (Specification: ¶¶ 122, 60).

50. The tag of claim of 47 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the phase of the coupling-means signal (Specification: ¶¶ 122, 56, 140);

a means for translating the weighted integration(s) into a bit value (Specification: ¶¶ 122. 60).

51. The tag of claim 47 wherein the first signal is a periodic signal with a first value for a predetermined signal parameter and the second signal is the periodic signal with a second value for the predetermined signal parameter, the predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the periodic signal, the bit-identifying means comprising:

a means for generating a first replica of the periodic signal with the first value for the predetermined signal parameter and a second replica of the periodic signal with the second value for the predetermined signal parameter (Specification: ¶¶ 122, 59);

a means for multiplying the coupling-means signal by the first replica thereby obtaining a first product waveform and by the second replica thereby obtaining a second product waveform

(Specification: ¶¶ 122, 59);

a means for integrating the first and second product waveforms for a bit period and translating the integration results into a bit value (Specification: ¶¶ 122, 59-60).

52. The tag of claim 47 wherein the first signal is a periodic signal with a first value for a first predetermined signal parameter and the second signal is the periodic signal with a second value for the first predetermined signal parameter, the first predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the periodic signal, the periodic signal modulating a second predetermined signal parameter of a carrier signal, the second predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the carrier signal, the bit-identifying means comprising:

a means for demodulating the second predetermined signal parameter of the coupling-means signal (Specification: ¶¶ 122, 49, 140);

a means for generating a first replica of the periodic signal with the first value for the first predetermined signal parameter and a second replica of the periodic signal with the second value for the first predetermined signal parameter (Specification: ¶¶ 122, 59, 140);

a means for multiplying the demodulated coupling-means signal by the first replica thereby obtaining a first product waveform and by the second replica thereby obtaining a second product waveform (Specification: ¶¶ 122, 59, 140);

a means for integrating the first and second product waveforms for a bit period and translating the integration results into a bit value (Specification: ¶¶ 122, 59-60, 140).

53. The tag of claim 47 wherein the bit-identifying means comprises:

a means for generating replicas of the first and second signals transmitted by the reader

(Specification: ¶¶ 115, 121);

a means for obtaining the amplitude of a coupling-means signal as a function of time (Specification: ¶ 112);

a means for multiplying the coupling-means signal amplitude by the replica of the first signal to obtain a first product signal and by the replica of the second signal to obtain a second product signal (Specification: ¶¶ 115, 121);

a means for integrating the first product signal over a bit period to obtain a first integration and integrating the second product signal over a bit period to obtain a second integration (Specification: ¶ 122);

a means for translating the first and second integrations into a bit value (Specification: ¶¶ 122, 60, 40).

54. The tag of claim 47 wherein the means for generating a bit-timing clock signal that indicates the start of each bit period comprises:

a means for generating a clock signal having a bit-start indicator during each bit period, the bit-start indicators being adjustable in time (Specification: ¶ 117);

a means for recognizing the bit transition in the coupling-means signal from one bit to the next (Specification: ¶ 115);

a means for adjusting the bit-start indicators until the bit-start indicators and the bit transitions in the coupling-means signal occur simultaneously (Specification: ¶¶ 118-119).

55. The tag of claim 47 wherein the reader embeds a bit-timing clock signal in the transmitted signals by initially alternating the transmission of the first signal and the second signal, the means for generating a bit-timing clock signal that indicates the start of each bit period

comprising:

a means for generating a clock signal having a bit-start indicator during each bit period, the bit-start indicators being adjustable in time (Specification: ¶ 117);

a means for recognizing the bit transitions in the coupling-means signal resulting from the transitions from the first signal to the second signal and from the second signal to the first signal (Specification: ¶ 115);

a means for adjusting the bit-start indicators until the bit-start indicators and the transitions in the coupling-means signal occur simultaneously (Specification: ¶¶ 118-119).

56. A tag for use with a reader, the reader transmitting a bit-timing clock signal to the tag, the tag comprising:

a coil (Specification: ¶ 39);

a capacitor (Specification: ¶ 39);

a means for coupling the capacitor to the coil (Specification: ¶ 39);

a means for driving the coil with a driving signal (Specification: ¶ 39);

a means for generating the driving signal (Specification: ¶ 39);

a means for generating a bit-timing clock signal synchronized to the reader bit-timing clock signal (Specification: ¶¶ 111-118);

a means for embedding a sequence of bits to be communicated to a reader in the driving signal, the start of each bit being controlled by the bit-timing clock signal (Specification: ¶ 124).

57. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal to have a first phase when a "0" bit is being transmitted and to have a second phase when a "1" bit is being transmitted (Specification: ¶

125).

58. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted (Specification: ¶¶ 125, 140).

59. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted (Specification: ¶¶ 125, 140).

60. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted (Specification: ¶¶ 125, 140).

61. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal to have a first frequency when a "0" bit is being transmitted and to have a second frequency when a "1" bit is being transmitted (Specification: ¶ 126).

62. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted (Specification: ¶¶ 126, 140).

63. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted (Specification: ¶¶ 126, 140).

64. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted (Specification: ¶¶ 126, 140).

65. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal (1) to have a first phase and a first frequency when a "00" bit pair is being transmitted, (2) to have a first phase and a second frequency when a "01" bit pair is being transmitted, (3) to have a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) to have a second phase and a second frequency when a "11" bit pair is being transmitted (Specification: ¶¶ 125-127).

66. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted (Specification: ¶¶ 125-127, 140).

67. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase

and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted (Specification: ¶¶ 125-127, 140).

68. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted (Specification: ¶¶ 125-127, 140).

69. The tag of claim 56 wherein the reader transmits the bit-timing clock signal to the tag by communicating a sequence of alternating "0" and "1" bits, a "0" bit being communicated by modulating the amplitude of the driving signal with a first periodic signal, a "1" bit being communicated by modulating the amplitude of the alternating field with a second periodic signal, the means for generating the clock signal that is synchronized to the bit-timing signal transmitted by the reader to the tag comprising:

a means for generating a clock signal having a bit-start indicator during each bit period, the bit-start indicators being adjustable in time (Specification: ¶ 117);

a means for obtaining the amplitude of a coupling-means signal as a function of time (Specification: ¶ 112);

a means for recognizing the transitions in the coupling-means signal amplitude at the time interfaces of the first and second periodic signals (Specification: ¶ 115);

a means for adjusting the bit-start indicators until the bit-start indicators and the transitions

in the coupling-means signal amplitude occur simultaneously (Specification: ¶¶ 118-119).

70. A method for interrogating a tag comprising the steps:

generating an alternating magnetic field (Specification: ¶¶ 30, 68-71);

embedding a bit-timing clock signal in the alternating magnetic field (Specification: ¶ 82);

embedding data to be communicated to a tag in the alternating magnetic field (Specification: ¶ 82).

71. A method for interrogating a tag, the tag responding to an interrogation by transmitting a sequence of bits, the start of each bit being determined by a bit-timing clock signal generated by the tag and synchronized with a bit-timing clock signal originating with the interrogator, the method comprising the steps:

generating a bit-timing clock signal (Specification: ¶ 51);

generating an alternating magnetic field in which the bit-timing clock signal is embedded (Specification: ¶¶ 30, 68-71, 82);

extracting data transmitted by the tag utilizing the bit-timing clock signal (Specification: ¶¶ 56-60).

72. A method of receiving a data sequence transmitted by a tag consisting of a message repeated a plurality of times, the message comprising a preamble, a tag data group of T bits, and an error-detecting group of E bits, the preamble consisting of a sync sequence of S bits, the tag data group and the error-detecting group possibly including false-sync sequences, the method comprising the steps:

receiving the data sequence transmitted by the tag (Specification: ¶¶ 56-62);

detecting each sync sequence in the received data sequence (Specification: ¶¶ 83-93);

identifying the preamble (Specification: ¶¶ 83-93);

extracting the tag data group from the received data sequence utilizing the identification of the preamble (Specification: ¶¶ 87, 91).

73. A method for responding to an interrogation by a reader, the method utilizing a resonating circuit comprising at least one capacitor coupled to a coil, the method comprising the steps:

driving the resonating circuit with a driving signal (Specification: ¶ 39);

maintaining the resonating circuit in resonance (Specification: ¶¶ 109-110);

embedding the sequence of bits to be communicated to the reader in the driving signal (Specification: ¶ 124).

74. A method for responding to the establishment of an alternating magnetic field by a reader, the reader embedding a bit-timing clock signal in the alternating magnetic field and communicating a sequence of bits by modulating the alternating magnetic field, the method comprising the steps:

deriving a signal from the alternating magnetic field (Specification: ¶ 40);

generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded in the alternating magnetic field (Specification: ¶¶ 111-118);

performing at least one weighted integration of the derived signal over a bit period using the bit-timing clock signal to identify the beginning and end of a bit period (Specification: ¶ 122);

identifying the bit being transmitted during each bit period utilizing the weighted integration(s) (Specification: ¶ 122).

75. A method for responding to the establishment of an alternating magnetic field by a

reader, a bit-timing signal being embedded in the alternating magnetic field by the reader, the method comprising the steps:

deriving a signal from the alternating magnetic field (Specification: ¶ 40);

generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded by the reader in the alternating magnetic field (Specification: ¶¶ 111-118);

generating an alternating magnetic field (Specification: ¶ 39);

modulating the alternating field generated by the responder with a sequence of bits to be communicated to a reader, the start of each transmitted bit being governed by the bit-timing clock signal (Specification: ¶ 124).

76. A method of communication between an interrogator and a responder, the method performed by the interrogator comprising the steps:

generating an alternating magnetic field (Specification: ¶¶ 30, 68-71);

embedding a bit-timing clock signal in the alternating magnetic field (Specification: ¶ 82);

extracting data communicated by the responder from an alternating magnetic field generated by the responder (Specification: ¶¶ 56-60);

the method performed by the responder comprising the steps:

extracting the bit-timing clock signal from the alternating magnetic field generated by the interrogator (Specification: ¶¶ 111-118);

generating a bit-timing clock signal that is synchronized to the bit-timing clock signal originating with the interrogator (Specification: ¶¶ 111-118);

generating an alternating magnetic field (Specification: ¶ 39);

embedding data to be communicated to the interrogator in the alternating magnetic field

generated by the responder, the start of each bit being controlled by the bit-timing clock signal generated by the responder (Specification: ¶ 124).

77. A method of communication between an interrogator and a responder, the method performed by the interrogator comprising the steps:

generating an alternating magnetic field (Specification: ¶¶ 30, 68-71);

embedding a bit-timing clock signal in the alternating magnetic field (Specification: ¶ 82);

embedding data to be communicated to the responder in the alternating magnetic field (Specification: ¶ 82);

the method performed by the responder comprising the steps:

extracting a bit-timing clock signal from the alternating magnetic field generated by the interrogator (Specification: ¶¶ 111-118);

performing at least one weighted integration of a signal derived from the alternating magnetic field generated by the interrogator over a bit period using the bit-timing clock signal to identify the beginning and end of a bit period (Specification: ¶ 122);

identifying the bit being transmitted during each bit period utilizing the weighted integration(s) (Specification: ¶ 122).

78. An apparatus for practicing the method of claim 73 (Specification: ¶¶ 39, 109-110, 124).

79. An apparatus for practicing the method of claim 76 (Specification: ¶¶ 30, 68-71, 82, 56-60, 111-118, 39,124).

80. An apparatus for practicing the method of claim 77 (Specification: ¶¶ 30, 68-71, 82, 111-118, 122).

ISSUES

I. Whether claims 20-24 are unpatentable under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement.

II. Whether claims 32 and 72 are unpatentable under 35 U.S.C. § 102(b) as being anticipated by Waraksa (U.S. 4,942,393).

III. Whether claims 36-40 are unpatentable under 35 U.S.C. § 102(e) in view of Buchele (U.S. 5,276,910).

IV. Whether claims 70,71, 73-80 are unpatentable under 35 U.S.C. § 102(e) in view of Carroll et al. (U.S. 5,517,194.

V. Whether claims 1, 3, 41, and 43 are unpatentable under 35 U.S.C. § 103(a) in view of Chatelot (U.S. 4,864,633) and Kurusu (U.S. 3,587,017).

VI. Whether claims 1, 2, 4, 41, 42, 44, and 45 are unpatentable under 35 U.S.C. § 103(a) in view of Chatelot (U.S. 4,864,633) and Ogita et al. (U.S. 4,278,980).

VII. Whether claims 5-13, 25, 47-60, and 62-64 are unpatentable under 35 U.S.C. § 103(a) in view of Carroll et al. (U.S. 5,517,194).

VIII. Whether claims 14-17, 61, and 64-68 are unpatentable under 35 U.S.C. § 103(a) in view of Carroll et al. (U.S. 5,517,194) and McFarlane (U.S. 3,223,779).

GROUPING OF CLAIMS

I. Insofar as Issue No. I is concerned: claims 20-22 stand or fall together;
claims 23-24 stand or fall separately;

II. Insofar as Issue No. II is concerned: claims 32 and 72 stand or fall separately;

III. Insofar as Issue No. III is concerned: claims 36 and 39 stand or fall together
claims 37, 38, and 40 stand or fall separately;

IV. Insofar as Issue No. IV is concerned: claims 70-71 and 73-80 stand or fall separately;

V. Insofar as Issue No. V is concerned: claims 1, 3, 41, and 43 stand or fall separately;

VI. Insofar as Issue No. VI is concerned: claims 1-2, 4, 41-42, and 44-45 stand or fall separately;

VII. Insofar as Issue No. VII is concerned: claims 5-13, 25, 47-60, and 62-64 stand of fall separately;

VIII. Insofar as Issue No. VIII is concerned: claims 14-17, 61, and 64-68 stand or fall separately.

ARGUMENT

I. WHETHER CLAIMS 20-24 ARE UNPATENTABLE UNDER 35 U.S.C. § 112, FIRST PARAGRAPH, AS FAILING TO COMPLY WITH THE ENABLEMENT REQUIREMENT.

CLAIMS 20-22

The examiner's specific basis for rejecting claims 20-24 is appellants' failure to describe in the specification specific "weighting functions" that might be used in the well-known "weighted integration" process: "Regarding claims 20-24, the specification does not describe the specific weighted integrations claimed. While weighted integrations may be well known in the art, the specific integrations claimed are not discussed in the present pecificationas required MPEP § 608.01(p) A." 01/15/04 Office Action, p. 2.

Claim 20 exemplifies the use of the term "weighted integration" in claims 20-22.

20. The reader of claim of 19 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the coupling-means signal;

a means for translating the weighted integration(s) into a bit value.

Claim 19, from which claims 20-22 depend, is based on resonance-tracking demodulator 15 (Specification: ¶¶ 56-62). The correlation-detection technology which provides the basis for the resonance-tracking demodulator 15 is described in numerous textbooks and handbooks. The means for identifying a received bit (Claim 19) is a correlation detector system consisting of balanced mixers 81 and 82 and sampled integrators 83 and 84 in Fig. 6 and the corresponding devices in Fig. 7. The balanced mixers provide the means for multiplying an amplitude-demodulated received signal with zero-phase, zero-average square wave C_{cm0} or C_{cm1} reference signals. Specification,

paragraphs 0058, 0059. The sampled integrators provide the integration means required in a correlation detector system.

A person skilled in the art would recognize that weighted integrations (as in claims 20-22) might be desirable for the purpose of suppressing intersymbol interference and the incorporation of such weights in the C_{cm0} or C_{cm1} reference signals is easily accomplished when the signals are generated by the VCO/CGC 13 (Fig. 1). This process, often referred to as "windowing", is also described in numerous textbooks and handbooks (see **ATTACHMENT I**, *Electronics Engineers' Handbook, Fourth Edition*, McGraw-Hill, New York, N.Y., 1997).

The examiner points out that the specification does not describe the specific weighted integrations claimed. Since specific weighting functions have been described, analyzed, and discussed extensively in the literature (see **ATTACHMENT II**, *The Industrial Electronics Handbook, IEEE Press*, 91-92, CRC Press LLC, Boca Raton, FL, 1997), it should not be necessary to repeat this material in the specification.

The examiner responded to the above arguments by stating:

"The applicants' conclusion is incorrect. All claimed subject matter must be supported by the disclosure" 01/15/04 Office Action, p. 8.

The examiner's statement is not supported by case law as reported in the Manual of Patent Examining Procedure:

> **"What is conventional or well known to one of ordinary skill in the art need not be disclosed in detail. See *Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d at 1367, 1384, 231 USPQ 81, 94, (Fed. Cir. 1986). If a skilled artisan would have understood the inventor to be in possession of the claimed invention at the time of filing, even if every nuance of the claims is not explicitly described in the specification, then the adequate description requirement is met." MPEP § 2163, II, A, 3, a.**

The test of enablement is whether a person skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation. *United States v. Telectronics, Inc.*, 857 F.2d 778, 785, 8 USPQ2d 1217, 1223 (Fed. Cir. 1988). As was pointed out above, knowledge of "weighted integrations" and specific "weighting functions" are well-known in the art, and it should not be necessary to repeat this information in the specification in order to meet the "enablement requirement".

Claims 20-22 fully meet the requirements of 35 U.S.C. § 112.

CLAIMS 23-24

Claims 23-24 do not involve the "weighted integration" process and the "weighted integration" term does not appear in the claim language. There appears to be no basis for the examiner's rejection of claims 23-24.

Claims 23-24 fully meet the requirements of 35 U.S.C. § 112.

II. WHETHER CLAIMS 32 AND 72 ARE UNPATENTABLE UNDER 35 U.S.C. § 102(B) AS BEING ANTICIPATED BY WARAKSA (U.S. 4,942,393).

CLAIM 32

Claim 32 reads as follows:

32. A reader for use with a tag that transmits a data sequence to the reader by repeating a message a plurality of times, ***[1] the message comprising a preamble, a tag data group of T bits, and an error-detecting group of E bits, the preamble consisting of a sync sequence of S bits, [2] the tag data group and the error-detecting group possibly including false-sync sequences****, the reader comprising:*

[3] a means for receiving the data sequence transmitted by the tag;

[4] a means for detecting each sync sequence in the received data sequence;

[5] a means for identifying the preamble;

[6] a means for extracting the tag data group from the received data sequence utilizing the identification of the preamble.

The limitations shown in bold face are not disclosed by Waraksa et al..

Limitation [1]

Claim 32 claims a reader which obtains data from a tag in the form of a message consisting of a plurality of bits, some of which constitute a "sync sequence" (limitation [1]). A "bit" is an abbreviation of "binary digit" and takes on one of two values, usually denoted as "0" or "1".

The communication of message bits from a tag to a reader requires the transformation of the message bits into analog waveforms that can be propagated electromagnetically by means of a carrier wave:

"The terminology 'line coding' originated in telephony with the need to transmit digital information across a copper telephone *line*; more specifically, binary data over a digital repeatered line. The concept of line coding, however readily applies to any transmission line or channel. In a digital communication system, there exists a known set of symbols to be transmitted. These can be designated as $\{m_i\}$, $i=1, 2, \ldots, N$, with a probability of occurrence $\{p_i\}$, $i=1, 2, \ldots, N$, where the sequentially traansmitted symbols are generally assumed to be statistically independent. The conversion or *coding* of these abstract symbols into real, temporal waveforms to be transmitted in baseband is the process of line coding." The Communications Handbook, Editor-in-Chief Jerry D. Gibson, CRC Press, Inc. Boca Raton, FL (1987) p. 386.

The most common transformation is to associate each bit in a message with one of two distinguishable analog waveforms, a "0" bit being associated with a "0" waveform and a "1" bit being associated with a "1" waveform. To receive the data sequence transmitted by a tag using the "0" and "1" waveforms, the reader must perform the inverse transformation by identifying the appropriate bit value to be associated with each of the received analog waveforms.

For example, let us assume that the "0" waveform is a constant voltage V_0 for the bit period and the "1" waveform is a constant voltage V_1 for the bit period. The transformation of the message bits into bit waveforms by the tag and the reverse transformation of the received bit waveforms into received message bits by the reader is very straightforward. It is so straightforward, in fact, that a person skilled in the art may feel it unnecessary to distinguish between bits and bit waveforms, referring to either a bit or its associated bit waveform as a bit. Since a bit and its associated bit waveform are in a one-to-one relationship, why not refer to either as being a "0" or a "1"? In many cases this short-hand way of referring to either a bit or its associated waveform is harmless. However, consider another example.

Again assume that the "0" waveform is a constant voltage V_0 for the bit period and the "1" waveform is a constant voltage V_1 for the bit period. In addition, after the bit waveforms have been

joined together into a message waveform, assume a "sync" waveform is added to the front end of the assembled message waveform by the tag to enable the reader to readily identify the beginning of a message waveform. And assume the "sync" waveform is a constant voltage V_0 maintained for the first half of a bit period and a constant voltage V_1 maintained for the second half of the bit period.

Note that the "sync" waveform is neither a "0" waveform nor a "1" waveform. It cannot be identified with either of the two bit values.

Waraksa et al., the prior art that the examiner asserts anticipates applicants' claim-32 invention, constitutes a second example of a "sync" waveform joined to a message waveform where the "sync" waveform cannot be represented by a bit or a bit sequence and consequently, cannot be said to be part of the "message", as defined in Limitation [1].

Limitation [1] specifies that a "message" be comprised of a "preamble" (consisting of a sync sequence of S bits), a tag data group of T bits, and an error-detecting group of E bits. Waraksa et al. discloses a "message" consisting of a 4- bit function code, a 20-bit identification code, and a 24-bit error correction code. Waraksa et al., col. 8, lines 46-58. Waraksa et al.'s "message" does not include a preamble consisting of a sync sequence and thus, does not disclose one of the limitations of claim 32.

After line coding the "message" using the Miller line code (*id.* at 395), Waraksa et al. adds a special line code (illegal under the Miller line code) to the beginning of the Miller encoded "message". Waraksa et al., col. 9, lines 52-55. The Miller waveforms associated with various bit combinations are shown in Fig. 3 of Waraksa et al.

The examiner argues that "Waraksa et al. discloses an S-bit sync sequence in the preamble as claimed." 01/15/04 Office Action, p. 9. As pointed out above, Waraksa et al.'s "SYNC pattern"

is an illegal Miller line code that is added to Waraksa et al.'s Miller encoded data word. Waraksa et al., col. 9, lines 34-36. Waraksa et al.'s "data word" corresponds to the claim-32 "message" and does not include a sync sequence. Waraksa et al.'s "data word" only contains a 4-bit function code, a 20-bit identification code, and a 24-bit ECC code. Waraksa et al., col. 9, lines 40-55.

The examiner argues that this preamble limitation can be ignored because "a preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone." 01/15/04 Office Action, p. 9.

The examiner was apparently highly influenced by the words "for use" in the limitation and too eagerly came to the conclusion that the limitation was MERELY a statement of use. The Manual of Patent Examining Procedure emphasizes:

> **"The claim preamble must be read in the context of the entire claim. The determination of whether preamble recitations are structural limitations or mere statements of purpose or use 'can be resolved only on review of the entirety of the [record] to gain an understanding of what the inventors actually invented and intended to encompass by the claim.' *Corning Glass Works v. Sumitomo Elec. U.S.A., Inc.*, 868 F.2d 1251, 1257, 9 USPQ2d 1962, 1966 (Fed. Cir. 1989)." MPEP § 2111.02.**

For example, the "for use" clause in "a bicycle for use in getting from one place to another" is merely a statement of use and does not imply any structural limitations on the bicycle. On the other hand, the "for use" clause in "a cell phone for use in the Verizon Wireless network" is not merely a statement of use but also implies certain structural limitations on the cell phone so that it has the capability of being used in the Verizon Wireless network.

In the case of the claim-32 preamble which specifies "A reader for use with a tag that communicates data to the reader by repeating a message a plurality of times, . . . ", the "for use" clause does not merely recite the intended use of a structure but includes the two structural limitations "[1] the message comprising a preamble consisting of a sync sequence of S bits, a tag data group of T bits, and an error-detecting group of E bits", and "[2] the data group and the error-detecting group possibly including false-sync sequences". The "for use" clause, like the cell phone example, is not merely a statement of use for a reader but also implies structural limitations on the reader to enable the reader to "read" messages produced by a tag. In such cases, the Manual of Patent Examining Procedure states:

> **"Any terminology in the preamble that limits the structure of the claimed invention must be treated as a claim limitation.** *See, e.g., Corning Glass Works v. Sumitomo Elec. U.S.A., Inc.*, **868 F.2d 1251, 1257, 9 USPQ2d 1962, 1966 (Fed. Cir. 1989);** *Pac-Tec Inc. v. Amerace Corp.*, **903 F.2d 796, 801, 14 USPQ2d 1871, 1876 (Fed. Cir. 1990).** *See also In re Stencel,* **828 F.2d 751, 4 USPQ2d 1071 (Fed. Cir. 1987)" MPEP § 2111.02.**

One might ask whether a reader for use with a tag that responds to a reader's interrogation with a message having a specified format asserts structural limitations that are not already fully and intrinsically set forth by the limitations in the body of the claim:

> **"If the body of a claim fully and intrinsically sets forth all of the limitations of the claimed invention, and the preamble merely states, for example, the purpose or intended use of the invention, rather than any distinct definition of any of the claimed invention's limitations, then the preamble is not considered a limitation and is of no significance to claim construction.** *Pitney Bowes, Inc. v. Hewlett-Packagd Co.*, **182 F.3d 1298, 1305, 51 USPQ2d 1161, 1165 (Fed. Cir. 1999)." MPEP § 2111.02.**

None of the body elements of the claims at issue disclose either separately or in combination Limitations [1] or [2], and thus, these limitations represent additional structural limitations which must be treated as legitimate claim limitations and not merely "a statement of purpose or use."

Limitation [2]

As claim 32 specifies, the tag repeats a message a number of times. A reader, when it starts receiving the message, does not know where the message begins. The sync sequence typically appears as the message preamble and thereby provides the means for the reader to identify the beginning of a message. There is a problem, however, in that the particular sequence chosen as the sync sequence may also appear by happenstance in the tag data group - error-correcting group portion of the message giving rise to a "false-sync" sequence and an erroneous indication of the beginning of the message. Thus, it is necessary to be able to distinguish in some fashion a "false-sync" sequence from a genuine "sync sequence", the genuine "sync sequence" being called the "preamble in claim 32. Limitation [2] points out the "false-sync" possiblility, and the necessity for the claimed apparatus being capable of recognizing a "false-sync" when it occurs.

Waraksa et al. uses a sync line code that is not a proper Miller line code and consequently avoids the possibility of the Miller line codes for a 4-bit sequence in the "message" producing a false sync:

> "As previously noted, it is necessary for the receiver to identify the beginning of the encoded transmission word and for this purpose a 4-bit SYNC pattern is added at the beginning of the code word which represents an illegal pattern for Miller encoding. Because of this illegal nature of the SYNC pattern, it can always be differentiated by the receiver from the code word." Waraksa et al., col. 6, line 66 - col. 7, line 4.

Note that the term "4-bit SYNC pattern" denotes a "SYNC pattern" that extends over a time period equivalent to that required to transmit the 4 Miller line codes for 4 "message" bits. Since the SYNC pattern is "an illegal pattern for Miller encoding", it is not the equivalent of 4 "message" bits.

Waraksa et al. does not disclose limitation [2] of claim 32.

The examiner argued in the 08/12/03 Office Action, pp. 12-13, that Limitation [2] is only a "possible feature, and as such is not interpreted as a positive limitation." The examiner modified his argument in the 01/15/04 Office Action, p. 9, to Limitation [2] being "an alternative feature, and as such is not interpreted as a positive limitation." How the examiner chooses to characterize Limitation [2] does not change the facts. The message received by appellants' reader may contain a "false-sync sequence" and the structure of appellants' reader must be able to distinguish between a genuine sync sequence and a "false-sync sequence"—a task not required of the Waraksa et al. invention since there is no such thing as a "false-sequence sequence" in the Waraksa et al. message.

The examiner also argues that this preamble limitation can be ignored because "the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. 01/15/04 Office Action, p. 9. The examiner is incorrect. The possibility of the tag data group and the error-detecting group including false-sync sequences is the only reason for including limitations [4] and [5] in the claim.

Limitation [3]

Limitation [3] specifies "a means for receiving the data sequence transmitted by the tag." The term "the data sequence transmitted by the tag" is defined in the preamble as a repeated message, "the message comprising a preamble consisting of a sync sequence of S bits, a tag data group of T bits, and an error-detecting group of E bits." Thus, "the data sequence transmitted by the tag" includes "a sync sequence of S bits."

The first definition of "receive" is "to have (something) given or conferred on one." *The Random House College Dictionary Revised Edition*, Random House, Inc., New York, N.Y., 1988.

Thus, "receiving the data sequence transmitted by the tag" means "to have the data sequence transmitted by the tag given or conferred on one." The term "data sequence" does not mean "line code modulated signals." Nor does it mean "line codes." The term "data sequence" means exactly what the preamble says it means: a repeated message, "the message comprising a preamble consisting of a sync sequence of S bits, a tag data group of T bits, and an error-detecting group."

Waraksa et al. discloses "receiving" data from a beacon by decoding the Miller encoded data. Waraksa et al., col. 17, lines 24-34. The Miller encoded data is a transform of a "data word" into Miller line codes, the "data word" consisting of a 24-bit MESSAGE and a 24-bit ECC code. Waraksa et al., col. 9, lines 29-39. There are no sync bits in Waraksa et al.'s "data word." Waraksa et al.'s SYNC pattern (an illegal Miller line code) is added later to the line codes associated with the "data word". Waraksa et al., col. 9, lines 34-36.

Since Waraksa et al.'s received "data word" does not contain "a sync sequence of S bits", Waraksa et al. does not disclose limitation [3], a means for receiving a message comprising a preamble consisting of a sync sequence of S bits, a tag data group of T bits, and an error-detecting group of E bits.

The examiner argued in the 08/12/03 Office Action, p. 13, that limitation [3] "does not set forth receiving sync data bits." However, the limitation states "a means for receiving the data sequence transmitted by the tag" and "the data sequence transmitted by the tag" includes a sync sequence of S bits as stated in the preamble of the claim.

The examiner also argued in the 08/12/03 Office Action, p. 13, that Waraksa et al. discloses receiving the Miller encoded code word and thereby discloses limitation [3], "receiving the data sequence transmitted by the tag." As we pointed out above, "data sequence" in claim 32 corresponds

to Waraksa et al.'s "code word" (Waraksa et al., col. 9, line 50). The "Miller encoded code word" are the joined-together line codes associated with the bits of the "code word". Thus, a Waraksa et al.'s disclosure of receiving the "Miller encoded code words" joined together with illegal Miller line codes for synchronization purposes is not a disclosure of receiving Waraksa et al.'s "code word" or appellants' "data sequence".

In the 01/15/04 Office Action, the examiner provided no rebuttal to the argument in the paragraph above and continued to insist that Waraksa et al.'s receiving of "Miller encoded code words" joined together with illegal Miller line codes for synchronization purposes were the same as receiving appellants' "data sequence".

Limitation [4]

Since Waraksa et al. does not disclose receiving a data sequence (Waraksa et al.'s "data word") that includes a sync sequence of S bits (see discussion under the ***Limitation [3]*** heading), Waraksa et al. obviously does not disclose limitation [4], "a means for detecting each sync sequence in the received data sequence."

The examiner argues: "The claim limitation is that the reader detects (not decodes) each sync sequence. Since the reader of Waraksa must detect the sync sequence in order for proper operation of the system, it reads on the claim." 01/15/04 Office Action, p. 10. The examiner omits five very important words (shown in boldface below) in limitation [4]: "a means for detecting each sync sequence **in the received data sequence.**" There is no sync sequence in Waraksa et al.'s received data sequence (see discussion under the ***Limitation [3]*** heading), and consequently, it would be have been pointless for Waraksa et al. to include a means in their invention to detect such sequences.

Limitation [5]

Limitation [1] specifies that a "message" be comprised of a "preamble" (consisting of a sync sequence of S bits), a tag data group of T bits, and an error-detecting group of E bits. Waraksa et al. discloses a "message" consisting of a 4- bit function code, a 20-bit identification code, and a 24-bit error correction code. Waraksa et al., col. 8, lines 46-58. Waraksa et al.'s "message" does not include a preamble consisting of a sync sequence and thus, does not disclose Limitation [1] of claim 32.

Since Waraksa et al. does not disclose receiving a data sequence (Waraksa et al.'s "data word") containing a message having a preamble consisting of a sync sequence of S bits (see discussion under the ***Limitation [3]*** heading), Waraksa et al. obviously does not disclose limitation [5], "a means for identifying the preamble."

The examiner argues that:

"The preamble of Waraksa includes the sync sequence. Because Waraksa detects the sync sequence, the preamble is identified." 01/15/04 Office Action, p. 10.

Waraksa et al. discloses a 48-bit "code word" consisting of a 4-bit function code, a 20-bit identification code, and 24 parity bits. Waraksa et al., col. 9, lines 40-50. There is no "preamble consisting of a sync sequence of S bits". (Waraksa et al. provides a sync means by appending an illegal Miller line code to the Miller line codes associated with the 48-bit "code word". Waraksa et al., col. 9, lines 52-55.) There is no "preamble consisting of a sync sequence of S bits" in Waraksa et al.'s "code word".

Limitation [6]

Since Waraksa et al. does not disclose receiving a data sequence containing a "message"

(Waraksa et al.'s "code word", col. 9, line 50), "the message comprising a preamble consisting of a sync sequence of S bits, a tag data group of T bits, and an error-detecting group of E bits" (see discussion under the ***Limitation [3]*** heading), Waraksa et al. obviously does not disclose limitation [6], "a means for extracting the tag data from the received data sequence utilizing the identification of the preamble."

The examiner argues that "Waraksa uses the sync sequence as a preamble to pre-empt the data sequence, therefore it is known by Waraksa that the data sequence follows the sync sequence." 01/15/04 Office Action, p. 11. Waraksa et al.'s illegal Miller line code is not a "preamble" as defined in claim 32. Waraksa et al. do not require a "preamble" in their "code word" to identify the beginning of the code word (the illegal Miller line codes serve to identify the beginning of the code word) and consequently, Waraksa et al. do not have nor do they require nor do they disclose the means for extracting data from the received "code word" utilizing the identification of the preamble.

> **"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference."** ***Verdegaal Bros. v. UnionOil Co. of California,*** **2 USPQ2d 1051, 1053 (Fed. Cir. 1987). (Cited in MPEP § 2131.)**

Waraksa et al. does not describe each and every element of claim 32 and therefore did not anticipate applicants' claim-32 invention.

Claim 32 is written in a means-plus-function format and is thus subject to the requirements of 35 U.S.C. § 112, sixth paragraph:

> **"As a consequence of a decision by the Court of Appeals for the Federal Circuit in its** ***en banc*** **decision** ***In re Donaldson Co.,*** **16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994), "examiners must interpret a 35 U.S.C. 112, sixth paragraph 'means or step plus**

function' limitation in a claim as limited to the corresponding structure, materials or acts described in the specification and equivalents thereof. . . ." MPEP § 2181.

Waraksa et al.'s digital data detector circuit 106 (Fig. 13a) detects the beginning of a message from the unique sync pattern, demodulates the PSK encoded signal, and supplies the resulting Miller encoded data to microcomputer 102. Waraksa et al., col. 11, lines 23-43.

The microcomputer 102 simply converts the Miller-encoded data into regular message bits, compares the message bits with data stored in memory, and based on the results of this comparison, controls the activation of various function. Waraksa et al., col. 11, lines 44-54.

What Waraksa et al. does not disclose is applicants' means for accomplishing limitations [3], [4], [5], and [6]. Applicants' embodiment of the means for accomplishing the aforementioned limitations is microprocessor 17 (Fig. 1) which performs the process shown in Fig. 10 (Specification, paragraphs 0085-0088) or the process shown in Fig. 11 (Specification, paragraphs 0089-0093). Waraksa et al., because of their use of a special "sync pattern" that cannot be duplicated by a sequence of ordinary message bits, does not have to search the received data for the beginning of the tag data. Applicants must examine the received data, bit by bit, to determine the beginning of the tag data.

There is no equivalency between the operations performed by Waraksa et al.'s digital data detector circuit 106 and microcomputer 102 and applicants' microprocessor 17, and consequently, Waraksa et al. did not anticipate applicants' claim 32 invention.

CLAIM 72

Claim 72 reads as follows:

72. *A method of receiving [1] a data sequence transmitted by a tag consisting of a message repeated a plurality of times, the message comprising a preamble, a tag data group of T bits, and an error-detecting group of E bits, the preamble consisting of a sync sequence of S bits, [2] the tag data group and the error-detecting group possibly including false-sync sequences, the method comprising the steps:*

[3] receiving the data sequence transmitted by the tag;

[4] detecting each sync sequence in the received data sequence;

[5] identifying the preamble;

[6] extracting the tag data group from the received data sequence utilizing the identification of the preamble.

The limitations of method claim 72 are essentially the same as those of apparatus claim 32. As discussed above under the *Claim 32* heading, Waraksa et al. does not disclose Limitations [1], [2], [3], [4], [5], and [6].

Waraksa et al. does not describe each and every element of claim 72 and therefore did not anticipate applicants' claim-72 invention.

Limitations [3] through [4] of claim 72 are step-plus-function limitations in that each of the limitations sets forth a step for reaching a particular result but not the specific technique or procedure used to achieve the result and are thus subject to the requirements of 35 U.S.C. 112, sixth paragraph. MPEP § 2181, *Caterpillar Inc. v. Detroit Diesel Corp.*, 41 USPQ2d 1876, 1882 (N.D. Ind. 1996).

Waraksa et al.'s digital data detector circuit 106 (Fig. 13a) detects the beginning of a message from the unique sync pattern, demodulates the PSK encoded signal, and supplies the resulting Miller encoded data to microcomputer 102. Waraksa et al., col. 11, lines 23-43.

The microcomputer 102 simply converts the Miller-encoded data into regular message bits, compares the message bits with data stored in memory, and based on the results of this comparison, controls the activation of various function. Waraksa et al., col. 11, lines 44-54.

What Waraksa et al. does not disclose is applicants' means for accomplishing Limitations [3], [4], [5], and [6] subject to Limitations [1] and [2]. Applicants' embodiment of the means for accomplishing the aforementioned limitations is microprocessor 17 (Fig. 1) which performs the process shown in Fig. 10 (Specification, paragraphs 0085-0088) or the process shown in Fig. 11 (Specification, paragraphs 0089-0093). Waraksa et al., because of their use of a special "sync pattern" that cannot be duplicated by a sequence of ordinary message bits, does not have to search the received data for the beginning of the tag data. Applicants must examine the received data, bit by bit, to determine the beginning of the tag data.

There is no equivalency between the operations performed by Waraksa et al.'s digital data detector circuit 106 and microcomputer 102 and applicants' microprocessor 17, and consequently, Waraksa et al. did not anticipate applicants' claim-72 invention.

III. WHETHER CLAIMS 36-40 ARE UNPATENTABLE UNDER 35 U.S.C. § 102(E) IN VIEW OF BUCHELE (U.S. 5,276,910).

CLAIMS 36 AND 39

Claim 36 reads as follows:

36. A reader for use with a tag, the reader comprising:

a coil;

[1] at least one capacitor;

[2] a means for coupling the capacitor(s) to the coil;

***[3] a means for driving the coil through the capacitor(s) with a driving signal,** the means consisting of four field-effect transistors connected in a bridge arrangement, two opposing junctions being connected to a power supply, the driving signal being available at the remaining two opposing junctions, the current flow through the transistors being controlled by a control signal applied to the gate of each transistor;*

a means for generating at least one control signal.

Limitation [1]

The examiner identifies capacitor 160 in Fig. 2 of Buchele as being the capacitor of limitation [1] which connects the "coupling means" of limitation [2] to the "driving means" of limitation [3] thereby allowing "driving signals" from the "driving means" to drive the coil. But capacitor 160 is a mere storage device for storing the energy available from a collapsing magnetic field. Buchele, col. 6, lines 41-47. Capacitor 160 does not connect Buchele's coil 190, either directly or through a coupling means, to the two opposing transistor junctions of Buchele's output driver 110 not

connected to a power supply as limitation [3] requires. The capacitor of limitation [1] does not exist in Buchele.

Limitation [2]

Limitation [2] of claim 36 is written in a means-plus-function format and is thus subject to the requirements of 35 U.S.C. 112, sixth paragraph:

> **"As a consequence of a decision by the Court of Appeals for the Federal Circuit in its en banc decision In re Donaldson Co., 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994), "examiners must interpret a 35 U.S.C. 112, sixth paragraph 'means or step plus function' limitation in a claim as limited to the corresponding structure, materials or acts described in the specification and equivalents thereof. . . ." MPEP § 2181.**

Applicants' means for coupling the capacitor(s) to the coil is shown in Fig. 1 as coupling circuit 7. Embodiments of coupling circuit 7 are shown in Figs. 2, 3, 4, and 5 and described in paragraphs 45, 46, and 47. In the direct connection of Fig. 2, one capacitor terminal connects to a terminal of coil 5 and the other capacitor terminal connects to a terminal of driver 11 (see Fig. 1). In the transformer coupling circuits of Figs. 3, 4, and 5, one capacitor terminal connects to a terminal of the primary winding and the other capacitor terminal connects to a terminal of driver 11 (see Fig. 1). The terminals of the secondary winding connect to coil 5.

In Buchele, the examiner identifies capacitor 160 as being coupled to coil 190 (Fig. 2). 01/15/04 Office Action, p. 3. However, capacitor 160 is not coupled to coil 190 either directly or by a transformer or an equivalent thereof. The connection of capacitor 160 across the source 170 of DC power for driver 110 does not constitute the coupling of capacitor 160 to coil 190.

Buchele does not disclose either the direct coupling or coupling through a transformer of capacitor 160 to coil 190 and consequently, did not anticipate limitation [1].

Limitation [3]

The Buchele's "H-bridge output driver 110" (Buchele, col. 5, lines 61-68) is the structural equivalent of the "bridge arrangement" specified in limitation [3]. Buchele's opposing junctions 146,156 and 124,134 are connected to a power supply (battery 170) just as limitation [3] specifies. Buchele's remaining two opposing junctions 136,144 and 126,154 are the source of the driving signal for coil 190 ("high power PWM signal", Buchele, col. 5, lines 46-52) just as limitation [3] specifies. The current flow through Buchele's H-bridge transistors are controlled by a control signal applied to the gate of each transistor (Buchele, col. 6, lines 21-40), just as limitation [3] specifies.

What Buchele does not disclose is the "high power PWM signal" (that exists at opposing junctions 136,144 and 126,154) feeding through capacitor(s) to coil 190. There are no capacitors in the lines connecting opposing junctions 136,144 and 126,154 to coil terminals 192 and 194. Thus, Buchele also does not disclose limitation [3].

Since Buchele does not disclose one or more limitations of claim 36, Buchele did not anticipate claim 36.

Buchele did not anticipate claim 39 because of its dependency on claim 36.

CLAIM 37

All of the transistors shown in Buchele's H bridge (Fig. 2) are n-channel devices. Buchele does not disclose the claim-37 limitation "wherein the bridge circuit comprises two series-connected P- and N-channel field effect transistors connected in parallel, the junction of the P devices and the

junction of the N devices being connected to a voltage supply, the driving signal being available at the junctions of the P and N devices."

Since Buchele does not disclose one or more limitations of claim 37, Buchele did not anticipate claim 37.

CLAIM 38

Buchele does not disclose in his H bridge (Fig. 2) "a diode connected between gate and source of each transistor to protect the gates from voltage spikes" and "a resistor in series with each gate of each transistor to suppress ringing in the gate circuit when the transistor is turned on."

Since Buchele does not disclose one or more limitations of claim 38, Buchele did not anticipate claim 38.

CLAIM 40

Buchele does not disclose in his H bridge (Fig. 2) "a two-winding transformer associated with each transistor, a control signal being fed into one winding of a transformer, the other winding being connected between gate and source electrodes of the associated transistor.

Since Buchele does not disclose one or more limitations of claim 40, Buchele did not anticipate claim 40.

IV. WHETHER CLAIMS 70,71, 73-80 ARE UNPATENTABLE UNDER 35 U.S.C. § 102(E) IN VIEW OF CARROLL ET AL. (U.S. 5,517,194.

CLAIM 70

Claim 70 reads as follows:

70. A method for interrogating a tag comprising the steps:

generating an alternating magnetic field;

embedding a bit-timing clock signal in the alternating magnetic field;

embedding data to be communicated to a tag in the alternating magnetic field.

Carroll et al. does not disclose the limitation in boldface.

Carroll et al. discloses controller 10 and transponder 40 which communicate with one another by performing the following steps:

- Controller 10 initiates communications by transmitting an unmodulated carrier (col. 9, lines 4-6);
- Transponder 40 receives the unmodulated carrier from controller 10, transmits a carrier obtained by dividing the frequency of the received unmodulated carrier by two (col. 13, lines 28-42), embeds a bit timing clock signal in the transmitted carrier (col. 14, lines 60-66; col. 20, lines 33-43)*, the embedded bit timing clock signal being obtained by further dividing down the frequency of the received unmodulated carrier to the bit rate (col. 12, lines 26-34), and embeds a data bit sequence in the transmitted carrier following the transmission of the embedded bit timing clock signal (col. 14, line 66 - col. 15, line 13);

- Controller 10 extracts the bit timing signal from the carrier received from transponder 40 (col. 15, lines 54-63), transmits data to transponder 40 in accordance with the bit timing signal received from transponder 40 (col. 16, lines 1-10, 46-52);**
- Transponder 40 extracts data from the carrier received from controller 10 using its own bit timing signal. Since controller 10's data was transmitted utilizing the bit timing clock signal supplied by transponder 40, there was no need for controller 10 to include a bit timing clock signal in its transmission to transponder 40.

* *Line coding is the process of converting or coding sequentially transmitted abstract symbols (such as "0" and "1") into real, temporal waveforms. Manchester line coding converts a "0" into a square wave that is negative during the first half of a bit period and positive during the second half. The Communications Handbook, Editor-in-Chief Jerry D. Gibson, CRC Press, Inc. Boca Raton, FL (1987) p. 386-394. A sequence of 4 "0's" results in a square wave having a frequency equal to the bit rate.*

** *The synchronization logic bits D0-D3 transmitted by controller 10 are a repetition of synchronization logic bits D0-D3 transmitted by transponder 40. Controller 10's synchronization bits do not result in the embedding of a bit-timing clock signal in controller 10's carrier because the controller 10 does not use Manchester line coding in transmitting data. To transmit a "0", controller 10 transmits a carrier having a frequency of 125 kHz for the entire bit period. To transmit a "1", controller 10 transmits a carrier having a frequency that shifts from 125 kHz to 116.3 kHz and back during a bit period (col. 16, lines 52-55). The transmission of the synchronization block consisting of 4 "0's" results in the transmission of a carrier having a frequency of 125 kHz for the entire 4-bit period.*

Thus, Carroll et al. does not disclose "embedding a bit-timing clock signal in the alternating magnetic field."

The examiner first argued that the synchronization block consisting of 4 "0's" which is transmitted by controller 10 constituted a bit-timing clock signal. 08/12/03 Office Action, p. 16. As we point out above, there is no bit timing information in the transmission of 4 "0's" by controller 10. Confirmation of this assertion is provided by the fact that Carroll et al. does not disclose

transponder 40 extracting a bit-timing clock signal from the signal received from controller 10. Carroll et al. only discloses a divide-by-64 timing control 60 which is simply a synchronous counter driven by the carrier received from controller 10 (col. 17, lines 39-51). Carroll et al. does disclose the extraction of a bit-timing clock signal by controller 10 (see Fig. 2E). Why would controller 10 need to extract the bit-timing clock signal from transponder 40's carrier if controller 10 had supplied the bit-timing clock signal to transponder 40 in the first place?

The examiner next argued that "The output of element 58 [see Carroll et al., Fig. 3] is a bit timing clock signal, the input to element 58 is the signal received from the reader, therefore, the clock signal is inherently embedded in the signal transmitted from the reader." 01/15/04 Office Action, p. 13. The output of amplifier 58 is NOT a bit timing signal. It is an FSK modulated data signal which ranges in frequency from 116.3 kHz to 125 kHz (see Carroll et al., Fig. 3). The timing control circuit 60 divides down this frequency, thereby generating a bit-timing clock signal Q6 which is used in transmitting data back to the reader. Carroll et al., col. 20, lines 33-43. Dividing down the frequency of an incoming carrier frequency is not the equivalent to extracting an embedded bit-timing clock signal from the carrier signal. The reader has no control over the zero crossings of the transponder-generated bit-timing clock signal since the reader cannot predict when the transponder will be powered up and the divide-by-64 timing control 60 will start operating.

The examiner also now argues that "Since Carroll's bit timing clock sequence provides timing for the bit clock 60 it meets the limitation claimed. 01/15/04 Office Action, p. 13. As we explained above, the transponder generates a bit-timing clock signal by dividing down the frequency of the received carrier. But this transponder-generated bit-timing clock signal is NOT a bit-timing clock signal that was embedded in the carrier by the reader.

The examiner's final argument is that "Assuming that the applicant is correct in stating that the bit timing signal is generated by the transponder 40, and the reader's data to the tag is synchronized with that bit timing signal, then the data from the reader to the tag has <u>embedded</u> data related to the bit timing signal. Again, as we explained above, the reader transmits data to the transponder that is synchronized to the bit-timing signal generated by the transponder and transmitted to the reader. But this process is not the same as the reader embedding a bit-timing clock signal in the alternating magnetic field which can then be extracted by the transponder for use in transmitting data to the reader.

Since Carroll et al. does not disclose at least one limitation of claim 70, Carroll et al. did not anticipate claim 70.

As a result of a Federal Circuit decision, examiners are required to interpret a step-plus-function limitation in a claim in terms of the corresponding structure, materials or acts described in the specification:

> **"As a consequence of a decision by the Court of Appeals for the Federal Circuit in its en banc decision In re Donaldson Co., 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994), "examiners must interpret a 35 U.S.C. 112, sixth paragraph 'means or step plus function' limitation in a claim as limited to the corresponding structure, materials or acts described in the specification and equivalents thereof. . . ." MPEP § 2181.**

The limitation "*embedding a bit-timing clock signal in the alternating magnetic field*" should be considered to be a step-plus-function element since "the element at issue sets forth a step for reaching a particular result, but not the specific technique or procedure used to achieve the result." *Caterpillar Inc. v. Detroit Diesel Corp.*, 41 USPQ2d 1876, 1882 (N.D. Ind. 1996) (cited in MPEP § 2181). Thus, this limitation is subject to the requirements of *In re Donaldson Co.*

The "embedding a bit-timing clock signal" step is accomplished by the circuitry shown in appellants' Fig. 8, as described in paragraph 0082 of appellants' specification, by microprocessor 17 transmitting an alternating sequence of "0's" and "1's", the bit-timing clock signal, upon the receipt of the "send message" command initiated by the user of the apparatus. Specification, ¶ 0081.

The acts and circuitry of Carroll et al., as described in col. 16, lines 1-10, 36-41, are quite different. Carroll et al.'s "controller 10" transmits data in bit-for-bit synchronization with the data received from "transponder 40". "Controller 10" repeats "sync block 102" (Carroll et al., Figs. 4A and 4B) but since it consists of 4 "0's" (no "0"-to-"1" transitions), it provides no useful bit-timing information to the transponder, and such information is not required by the transponder in any event since the data transmitted by "controller 10" is bit-synchronized to the data transmitted by "transponder 40" to the controller.

An *In re Donaldson Co.* analysis comes to the same conclusion as a straightforward analysis of the words of the claim. Carroll et al. does not disclose the "embedding a bit-timing clock signal in the alternating magnetic field" limitation of claim 70 and did not anticipate claim 70.

CLAIM 71

Claim 71 reads as follows:

71. A method for interrogating a tag, [1] the tag responding to an interrogation by transmitting a sequence of bits, the start of each bit being determined by a bit-timing clock signal generated by the tag and synchronized with a bit-timing clock signal originating with the interrogator, the method comprising the steps:

[2] generating a bit-timing clock signal;

[3] generating an alternating magnetic field in which the bit-timing clock signal is embedded;

[4] extracting data transmitted by the tag utilizing the bit-timing clock signal.

Carroll et al. does not disclose any of the four limitations shown in boldface.

Limitation [1]

Carroll et al.'s transponder 40 responds to an interrogation by transmitting a sequence of bits in accordance with a bit-timing clock signal generated by transponder 40, but the bit-timing clock signal is NOT synchronized with a bit-timing clock signal originating from controller 10 since controller 10 does NOT transmit a bit-timing clock signal to transponder 40.

Carroll et al.'s bit-timing clock in transponder 40 is obtained by dividing down the frequency of the interrogating signal. Carroll et al., col. 12, line 20 - col. 13, line 7. As discussed above under the *Claim 70* heading, controller 10 does not transmit a bit-timing clock signal to transponder 40, and transponder 40 does not require one.

The examiner argues that "The sync signal that is generated in element 70 of Carroll is a bit timing clock signal." 01/15/04 Office Action, p. 14. Element 70 is a "Manchester Encoder and Sync Generator" located in Carroll et al.'s transponder 40 and reinforces appellants' position that bit-timing for data transmission in Carroll et al.'s invention originates in "transponder 40".

The examiner argues that limitation [1] appears in the preamble of the claim and merely recites the purpose of a process. 01/15/04 Office Action, p. 14. However, *The Manual of Patent Examining Procedure* emphasizes:

> **"Any terminology in the preamble that limits the structure of the claimed invention must be treated as a claim limitation. See, e.g. *Corning Glass Works v. Sumitomo Elec.***

U.S.A., Inc., 868 F.2d 1251, 1257, 9 USPQ2d 1962, 1966 (Fed. Cir. 1989)." MPEP § 2111.02.

In the case of a method claim, it would be appropriate to substitute "steps" for "structure". For example, "a method for getting from one place to another" is merely a statement of the purpose of the method and does not imply any limitations on the method steps. On the other hand, "a method for communicating using the Verizon Wireless network" is not merely a statement of use but also implies certain limitations on the method steps if the method steps are to be compatible with the Verizon Wireless network.

In the present case of a method for interrogating a tag which responds "to an interrogation by transmitting a sequence of bits, the start of each bit being determined by a bit-timing clock signal generated by the tag and synchronized with a bit-timing clock signal originating with the interrogator", the "for use" clause, like the cell phone example, is not merely a statement of use but also implies limitations on the method steps if the method steps are to be compatible with tags having the specified characteristics. Consider, for example, the consequences of omitting "and synchronized with a bit-timing clock signal originating with the interrogator." Such an omission would have a profound effect on the scope of limitation [4] since extracting data transmitted by the tag would be significantly more complicated if the bit-timing clock signals of interrogator and tag were not synchronized.

This example demonstrates that limitation [1] affects the scope of at least one of the other limitations and must be taken into account in determining the patentability of the claim.

One might ask whether a method for interrogating a tag which responds "to an interrogation by transmitting a sequence of bits, the start of each bit being determined by a bit-timing clock signal

generated by the tag and synchronized with a bit-timing clock signal originating with the interrogator" asserts step limitations that are not already fully and intrinsically set forth by the limitations in the body of the claim:

> **"If the body of a claim fully and intrinsically sets forth all of the limitations of the claimed invention, and the preamble merely states, for example, the purpose or intended use of the invention, rather than any distinct definition of any of the claimed invention's limitations, then the preamble is not considered a limitation and is of no significance to claim construction. *Pitney Bowes, Inc. v. Hewlett-Packagd Co.*, 182 F.3d 1298, 1305, 51 USPQ2d 1161, 1165 (Fed. Cir. 1999)." MPEP § 2111.02.**

None of the body elements of the claims at issue disclose either separately or in combination limitation [1] and thus, this limitation represents an additional limitation which must be treated as a legitimate claim limitation and not merely "a statement of purpose or use."

Limitation [2]

Carroll et al.'s controller 10 does not generate a bit-timing clock signal which, as the claim preamble specifies, is the bit-timing reference for both controller 10 and transponder 40. Carroll et al.'s transponder 40 generates a bit-timing clock signal and transmits it to controller 10 as sync block 102 in configuration word 100 (Fig. 4A). Sync block 102 consists of four "0's" which, after being converted to Manchester line codes, become a square wave having a frequency equal to the bit rate. This square wave is used by controller 10 as the bit-timing clock signal in extracting the other parts 106, 108, and 110 of configuration word 100 from the carrier transmitted by transponder 40.

Controller 10 transmits command word 112 in bit for bit synchronization with configuration word 100 including sync block 114 consisting of four "0's" (Fig. 4B, col. 16, lines 1-10). Controller 10 does not use Manchester line codes, however, and the four "0's" are not converted to the square-wave bit-timing clock signal as was the case with transponder 40's transmission. Instead, each "0"

becomes a carrier lasting for the bit period with a frequency of 125 kHz. (A "1" is transmitted by toggling the carrier frequency between 125 kHz and 116.3 kHz (col. 11, lines 11-26).) Four "0's" becomes a carrier lasting for four bit periods with a frequency of 125 kHz.

Thus, there is no bit-timing information available in controller 10's transmission of four "0's" nor would one expect there to be since a bit-timing clock signal already exists in transponder 40. Controller 10 neither generates a bit-timing clock signal nor does it transmit the bit-timing clock signal it receives from transponder 40 back to transponder 40.

The examiner argues that "[t]he sync signal that is generated in element 70 of Carroll is a bit timing clock signal." 01/15/04 Office Action, p.14. The sync signal referred to by the examiner has to do with acts performed in transponder 40. Limitation [2] refers to an act performed by the "interrogator", the counterpart in Carroll et al. being controller 10. Controller 10 does not generate a bit-timing clock signal.

Limitation [3]

Carroll et al.'s controller 10 does not embed a bit-timing clock signal in the interrogating signal transmitted to transponder 40. Please see discussion above under the **CLAIM 70** heading.

The examiner argues that "[t]he sync signal that is generated in element 70 of Carroll is a bit timing clock signal and is transmitted through the PSK modulator." 01/15/04 Office Action, p. 14. The sync signal referred to by the examiner has to do with acts performed in transponder 40. Limitation [3] refers to an act performed by the "interrogator", the counterpart in Carroll et al. being controller 10. Controller 10 does not generate an alternating magnetic field in which the bit-timing clock signal is embedded.

Limitation [4]

Carroll et al.'s controller 10 does not extract the data carried by the signal transmitted by transponder 40 using a bit-timing signal originating in controller 10. Carroll et al.'s controller 10 does not generate such a signal (see discussion above under ***Limitation [2]*** heading) and obviously cannot use it in extracting the data sent by transponder 40.

Carroll et al. does not describe each and every element of claim 71 and therefore did not anticipate appellants' claim-71 invention.

As a result of a Federal Circuit decision, examiners are required to interpret means-plus-function and step-plus-function limitations in a claim in terms of the corresponding structure, materials or acts described in the specification:

> **"As a consequence of a decision by the Court of Appeals for the Federal Circuit in its en banc decision In re Donaldson Co., 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994), "examiners must interpret a 35 U.S.C. 112, sixth paragraph 'means or step plus function' limitation in a claim as limited to the corresponding structure, materials or acts described in the specification and equivalents thereof. . . ." MPEP § 2181.**

Limitation [1] should be considered to be a means-plus-function claim since it recites a function to be performed and does not recite sufficient structure to preclude application of 35 U.S.C. § 112, sixth paragraph. Limitations [2], [3], and [4] should be considered to be step-plus-function elements since "the element at issue sets forth a step for reaching a particular result, but not the specific technique or procedure used to achieve the result." *Caterpillar Inc. v. Detroit Diesel Corp.*, 41 USPQ2d 1876, 1882 (N.D. Ind. 1996) (cited in MPEP § 2181). Thus, all of the boldface limitations are subject to the requirements of *In re Donaldson Co.*

With respect to limitation [1], paragraphs 0111 through 0119 of the specification, with reference to Fig. 18, describe how a bit-timing clock signal generated by the tag is synchronized with a bit-timing clock signal originating with the interrogator. The bit-timing clock signal is generated by frequency divider 255 and frequency divider 281 which divides down the frequency of the received signal.

Carroll et al. uses timing control 60 in Fig. 5 to generate a bit-timing signal. But there is nothing in Carroll et al.'s Fig. 5 that corresponds to appellants' Fig. 18 circuitry that extracts an embedded bit-timing clock signal from the interrogating magnetic field and then synchronizes the generated bit-timing clock signal with the extracted bit-timing clock signal.

With respect to Limitations [2] and [3], the bit-timing clock signal is generated in appellants' reader by VCO/CGC 13. Specification, ¶ 0051. The bit-timing clock signal is embedded in the alternating magnetic field by the circuitry shown in appellants' Fig. 8, as described in paragraph 0082 of appellants' specification, by microprocessor 17 transmitting an alternating sequence of "0's" and "1's" upon the receipt of the "send message" command initiated by the user of the apparatus. Specification, ¶ 0081.

Carroll et al. describes in detail the operations performed by microcomputer 12 beginning at col. 7, line 5, but does NOT disclose the generation of a bit-timing clock signal. Carroll et al. describes the generation of an "RF magnetic field" by microprocessor 12 (col. 7, lines 5-10), but Carroll et al. does NOT disclose embedding a bit-timing clock signal in the RF magnetic field. Carroll et al. describes how the "start" bit of transponder 40's message is identified (col. 10, lines 53-61), but Carroll et al. does NOT disclose extracting data transmitted by transponder 40 utilizing a bit-timing clock signal.

An *In re Donaldson Co.* analysis comes to the same conclusion as a straightforward analysis of the words of claim 71. Carroll et al. does not disclose any of limitations [1]-[4] and did not anticipate claim 71.

CLAIM 73

Claim 73 reads as follows:

73. A method for responding to an interrogation by a reader, the method utilizing a resonating circuit comprising at least one capacitor coupled to a coil, the method comprising the steps:

driving the resonating circuit with a driving signal;

maintaining the resonating circuit in resonance;

embedding the sequence of bits to be communicated to the reader in the driving signal.

Carroll et al. does not disclose the limitation shown in boldface. Carroll et al. discloses the use of a resonating circuit which is tuned to the frequency of the interrogating signal. Carroll et al., col. 12, lines 1-19. Nothing is said about maintaining the resonating circuit in resonance.

The examiner argues that maintaining the resonating circuit in resonance "is inherent to any receiver that is attempting to receive data on a carrier (which Carroll does)." 01/15/04 Office Action, p. 15. The examiner is incorrect. Maintaining the resonating circuit in resonance is NOT inherent to any receiver that is attempting to receive data on a carrier. The examiner was obligated to supply evidence of inherency and did not do so:

> **"To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic**

> **evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill."** ***Continental Can Co. USA v. Monsanto Co.*****, 948 F.2d, 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991).**

Carroll et al. does not describe each and every element of claim 73 and therefore did not anticipate applicants' claim-73 invention.

As a result of a Federal Circuit decision, examiners are required to interpret a step-plus-function limitation in a claim in terms of the corresponding structure, materials or acts described in the specification:

> **"As a consequence of a decision by the Court of Appeals for the Federal Circuit in its en banc decision In re Donaldson Co., 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994), "examiners must interpret a 35 U.S.C. 112, sixth paragraph 'means or step plus function' limitation in a claim as limited to the corresponding structure, materials or acts described in the specification and equivalents thereof . . . ." MPEP § 2181.**

The limitation "***maintaining the resonating circuit in resonance***" should be considered to be a step-plus-function element since "the element at issue sets forth a step for reaching a particular result, but not the specific technique or procedure used to achieve the result." *Caterpillar Inc. v. Detroit Diesel Corp.*, 41 USPQ2d 1876, 1882 (N.D. Ind. 1996) (cited in MPEP § 2181). Thus, this limitation is subject to the requirements of *In re Donaldson Co.*

The "maintaining the resonating circuit in resonance" step is accomplished by frequency-modulating the driving frequency with a square wave in the reader (Specification: ¶¶ 0048, 0108; Figs. 1, 6). The frequency-modulated driver is used in the tag to maintain the resonant circuit in or near resonance (Specification: ¶¶ 0109-110; Figs. 1, 18). There is no comparable circuitry disclosed in Carroll et al.

An *In re Donaldson Co.* analysis comes to the same conclusion as a straightforward analysis of the words of the claim. Carroll et al. does not disclose appellants' circuitry for "maintaining the resonating circuit in resonance", or equivalents thereof and consequently did not anticipate appellants' claim-73 invention.

CLAIM 74

Claim 74 reads as follows:

*74. A method for responding to the establishment of an alternating magnetic field by a reader, **[1] the reader embedding a bit-timing clock signal in the alternating magnetic field** and communicating a sequence of bits by modulating the alternating magnetic field, the method comprising the steps:*

deriving a signal from the alternating magnetic field;

[2] generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded in the alternating magnetic field;

[3] performing at least one weighted integration of the derived signal over a bit period using the bit-timing clock signal to identify the beginning and end of a bit period;

[4] identifying the bit being transmitted during each bit period utilizing the weighted integration(s).

Carroll et al. does not disclose any of the limitations shown in boldface.

Limitation [1]

This limitation is the same as the boldface limitation of claim 70. Please see the argument presented above under the CLAIM 70 heading in support of the assertion that Carroll et al. does not disclose "embedding a bit-timing clock signal in the alternating magnetic field".

The examiner states that this limitation, since it appears in the preamble of the claim, was not "given patentable weight." 01/15/04 Office Action, p. 15. However:

> **"If the claim preamble, when read in the context of the entire claim, recites limitations of the claim, or, if the claim preamble is 'necessary to give life, meaning, and vitality' to the claim, then the claim preamble should be construed as if in the balance of the claim."** ***Pitney Bowes, Inc. v. Hewlett-Packard Co.*****, 182 F.3d 1298, 1305, 51 USPQ2D 1161, 1165-66 (Fed. Cir. 1999).**

Certainly, the preamble in the present case is necessary to give meaning to the body limitations of the claim and "should be construed as if in the balance of the claim."

Limitation [2]

Carroll et al. does not disclose "generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded in the alternating magnetic field". There is no bit-timing clock signal embedded in the alternating magnetic field created by Carroll et al.'s controller 10 (see discussion under the CLAIM 70 heading), and consequently, there is no way for transponder 40 to generate a bit-timing clock signal "that is synchronized to the bit-timing clock signal embedded in the alternating magnetic field". Note that the only clock signal available to Carroll et al.'s "divide-by-64" timing control 60 (Fig. 3), which supplies all the timing signals for transponder 40, is the incoming FSK modulated data signal. Carroll et al., col. 12, lines 20-25. The "divide-by-64" timing control 60 is nothing more than a digital counter. Carroll et al., col. 12, lines 26-34. One of the

outputs of timing control 60 is Q6 which is the bit-timing clock signal generated by transponder 40 and used in transmitting data to controller 10. Carroll et al., col. 18, lines 53-57; col. 20, lines 33-43. Q6 has the proper bit-timing frequency of 1.953 kHz, but its zero-crossings are determined by how long it takes to power-up transponder 40 and have timing control 60 start to operate. There is no bit-timing clock signal available in the alternating magnetic field to which the zero crossings of Q6 could be synchronized. Nothing is said in Carroll et al. about synchronizing Q6 to an embedded bit-timing signal.

The examiner states that "applicant argues (2) that the bit timing clock signal is not synchronized to the bit timing clock signal from the interrogator." 01/15/04 Office Action, p. 15. This is not a correct statement of appellants' argument. Appellants argue that there is no bit-timing clock signal available from controller 10, and consequently, it would be impossible for transponder 40 to synchronize its locally-generated bit-timing clock signal with a non-existent bit-timing clock signal from controller 10.

The examiner argues that "[t]he sync generator 70 is synchronized to the received clock signal since the timing control element 60 drives all the elements that follow, etc 64,48,68 and 70." 01/15/04 Office Action, p. 16. The "received clock signal" that the examiner refers to is presumably the FSK modulated signal of frequency 125 kHz from controller 10. col. 7, lines 22-25; col. 17, lines 39-52. This is the carrier of the data that controller 10 transmits to transponder 40. It carries no information as to the timing of the zero crossings of the bit-timing clock signal, and consequently is not a bit-timing clock signal to which the bit-timing clock signal generated by transponder 40 can be synchronized.

As we have emphasized repeatedly, controller 10 does NOT provide a bit-timing clock signal to which transponder 40's locally-generated bit-timing clock signal could be synchronized.

Carroll et al. does not disclose limitation [2].

As a result of a Federal Circuit decision, examiners are required to interpret a step-plus-function limitation in a claim in terms of the corresponding structure, materials or acts described in the specification:

> **"As a consequence of a decision by the Court of Appeals for the Federal Circuit in its en banc decision In re Donaldson Co., 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994), "examiners must interpret a 35 U.S.C. 112, sixth paragraph 'means or step plus function' limitation in a claim as limited to the corresponding structure, materials or acts described in the specification and equivalents thereof. . . ." MPEP § 2181.**

The limitation ***"generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded in the alternating magnetic field"*** should be considered to be a step-plus-function element since "the element at issue sets forth a step for reaching a particular result, but not the specific technique or procedure used to achieve the result." *Caterpillar Inc. v. Detroit Diesel Corp.*, 41 USPQ2d 1876, 1882 (N.D. Ind. 1996) (cited in MPEP § 2181). Thus, this limitation is subject to the requirements of *In re Donaldson Co.*

"Generating a bit-timing clock signal" is accomplished by appellants' frequency divider 255 and frequency divider 281 as shown in Fig. 18 and described in the Specification, ¶ 0117. The embedded bit-timing clock signal is extracted from the received interrogating signal by amplitude demodulator 251 and used to synchronize the generated bit-timing signal as described in the Specification, ¶ 0118. There is nothing in Carroll et al. that corresponds to appellants' synchronization circuitry as shown in appellants Fig. 18 and described in paragraph 0118 of the Specification.

An *In re Donaldson Co.* analysis comes to the same conclusion as a straightforward analysis of the words of the claim. Carroll et al. does not disclose appellants' circuitry for "generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded in the alternating magnetic field", or equivalents thereof, and consequently did not anticipate Limitation [2] of appellants' claim-74 invention.

Limitation [3]

There is nothing in Carroll et al. that is even suggestive of Limitation [3].

The examiner states that "applicant argues (3) that Carroll does not use weighted integration to identify the bit period." 01/15/04 Office Action, p. 16. Appellants do not make this argument. Appellants argue that Carroll et al. do not disclose limitation [3] which specifies "performing at least one weighted integration of the derived signal over a bit period USING THE BIT-TIMING CLOCK SIGNAL TO IDENTIFY THE BEGINNING AND END OF A BIT PERIOD."

The examiner argues that [d]ividing by 64 is weighted integration for providing the claimed feature. The divide-by-64 timing control 60 is simply a synchronous counter (col. 18, lines 58-60). It has nothing to do with performing a weighted integration of a received signal. A weighted integration results from the multiplication of the signal received during a bit period by a weighting function and integrating the result.

Carroll et al. does not disclose limitation [3].

As a result of a Federal Circuit decision, examiners are required to interpret a step-plus-function limitation in a claim in terms of the corresponding structure, materials or acts described in the specification:

> **"As a consequence of a decision by the Court of Appeals for the Federal Circuit in its en banc decision In re Donaldson Co., 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994), "examiners must interpret a 35 U.S.C. 112, sixth paragraph 'means or step plus function' limitation in a claim as limited to the corresponding structure, materials or acts described in the specification and equivalents thereof. . . ." MPEP § 2181.**

The limitation ***"performing at least one weighted integration of the derived signal over a bit period using the bit-timing clock signal to identify the beginning and end of a bit period"*** should be considered to be a step-plus-function element since "the element at issue sets forth a step for reaching a particular result, but not the specific technique or procedure used to achieve the result." *Caterpillar Inc. v. Detroit Diesel Corp.*, 41 USPQ2d 1876, 1882 (N.D. Ind. 1996) (cited in MPEP § 2181). Thus, this limitation is subject to the requirements of *In re Donaldson Co.*

Limitation [3] is accomplished in appellants' invention by means of balanced mixers 259 and 260 and sampled integrators 282 and 284 (see Fig. 18) in the same way as the similar task was accomplished in the reader with balanced mixers 81 and 82 and sampled integrators 83 and 84 (see Fig. 6). Specification, ¶ 0122. Carroll et al. identify FSK detector 64 (consisting e.g. of an internal oscillator, a four bit up/down counter and the logic necessary to determine the relative input frequencies of the FSK modulated RF signal output from the controller 10) as the means for extracting the data transmitted by controller 10 to transponder 40. Carroll et al., col. 12, lines 26-34, col. 18, lines 47-53.

Carroll et al.'s FSK detector 64 is not an equivalent of appellants' balanced mixer/sampled integrator circuit.

An *In re Donaldson Co.* analysis comes to the same conclusion as a straightforward analysis of the words of the claim. Carroll et al. does not disclose appellants' circuitry for "performing at least one weighted integration of the derived signal over a bit period using the bit-timing clock signal to

identify the beginning and end of a bit period", or equivalents thereof, and consequently did not anticipate Limitation [3] of appellants' claim-74 invention.

Limitation [4]

Carroll et al. does not disclose "weighted integrations" and obviously does not disclose the use of weighted integrations in identifying the bit being transmitted.

The examiner stated in his 08/12/03 Office Action that "[e]lement 62 [Carroll et al.'s Fig. 3] does use the weighted integration to identify the incoming data." 08/12/03 Office Action, p. 18. Element 62 is an "address register" used to access the selected bits within the words of the non-volatile memory array (col. 18, lines 14-17). This "address register" has nothing to do with identifying the bit being transmitted during each bit period. Carroll et al.'s FSK detector 64 identifies the bit being transmitted simply by measuring the frequency of the FSK modulated signal output from controller 10 (col. 18, lines 44-57). No weighted integrations are involved.

In his 01/15/04 Office Action the examiner elaborated on his "element 62" statement:

> "The examiner has emphasized repeatedly that the applicant's claims are not as narrow as they argue. The claims do not require that the bit-timing signal be "originated" by the reader, merely that the signal from the reader includes some embedded bit timing signal. Since the reader sends data synchronized using the bit-timing signal the applicant argues is originated by the transponder, the data from the reader includes embedded bit timing signal information." 01/15/04 Office Action, p. 16.

This comment by the examiner has nothing to do with limitation [4], "identifying the bit being transmitted during each bit period utilizing the weighted integration(s)."

As a result of a Federal Circuit decision, examiners are required to interpret a step-plus-function limitation in a claim in terms of the corresponding structure, materials or acts described in the specification:

> **"As a consequence of a decision by the Court of Appeals for the Federal Circuit in its en banc decision In re Donaldson Co., 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994), "examiners must interpret a 35 U.S.C. 112, sixth paragraph 'means or step plus function' limitation in a claim as limited to the corresponding structure, materials or acts described in the specification and equivalents thereof. . . ." MPEP § 2181.**

The limitation "***identifying the bit being transmitted during each bit period utilizing the weighted integration(s)***" should be considered to be a step-plus-function element since "the element at issue sets forth a step for reaching a particular result, but not the specific technique or procedure used to achieve the result." *Caterpillar Inc. v. Detroit Diesel Corp.*, 41 USPQ2d 1876, 1882 (N.D. Ind. 1996) (cited in MPEP § 2181). Thus, this limitation is subject to the requirements of *In re Donaldson Co.*

Limitation [4] is accomplished in appellants' invention by using microprocessor 61 to compare the magnitudes of the weighted-integration outputs of sampled integrators 282 and 284 (see Fig. 18). Specification, ¶ 0122. Carroll et al. identify FSK detector 64 (consisting e.g. of an internal oscillator, a four bit up/down counter and the logic necessary to determine the relative input frequencies of the FSK modulated RF signal output from the controller 10) as the means for extracting the data transmitted by controller 10 to transponder 40. Carroll et al., col. 12, lines 26-34, col. 18, lines 47-53.

Carroll et al.'s FSK detector 64 does not compare weighted integrations and is therefore not an equivalent of appellants' balanced mixer/sampled integrator/microprocessor circuit.

An *In re Donaldson Co.* analysis comes to the same conclusion as a straightforward analysis of the words of the claim. Carroll et al. does not disclose appellants' circuitry for "identifying the bit being transmitted during each bit period utilizing the weighted integration(s)", or equivalents thereof, and consequently did not anticipate limitation [4] of appellants' claim-74 invention.

Carroll et al. does not describe each and every element of claim 74 and therefore did not anticipate applicants' claim-74 invention.

CLAIM 75

Claim 75 reads as follows:

75. A method for responding to the establishment of an alternating magnetic field by a reader, ***[1] a bit-timing signal being embedded in the alternating magnetic field by the reader,*** *the method comprising the steps:*

deriving a signal from the alternating magnetic field;

[2] generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded by the reader in the alternating magnetic field;

generating an alternating magnetic field;

[3] modulating the alternating field generated by the responder with a sequence of bits to be communicated to a reader, the start of each transmitted bit being governed by the bit-timing clock signal.

Carroll et al. does not disclose any of the limitations shown in boldface.

Limitation [1]

This limitation is the same as the boldface limitation of claim 70. Please see the argument presented above under the **CLAIM 70** heading in support of the assertion that Carroll et al. does not disclose "embedding a bit-timing clock signal in the alternating magnetic field".

The examiner states that this limitation, since it appears in the preamble of the claim, was not "given patentable weight." 01/15/04 Office Action, p. 15. However:

> **"If the claim preamble, when read in the context of the entire claim, recites limitations of the claim, or, if the claim preamble is 'necessary to give life, meaning, and vitality' to the claim, then the claim preamble should be construed as if in the balance of the claim."** ***Pitney Bowes, Inc. v. Hewlett-Packard Co.*****, 182 F.3d 1298, 1305, 51 USPQ2D 1161, 1165-66 (Fed. Cir. 1999).**

Certainly, the preamble in the present case is necessary to give meaning to the body limitations of the claim and "should be construed as if in the balance of the claim."

Limitation [2]

Carroll et al. does not disclose "generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded in the alternating magnetic field". Limitation [2] of claim 74 is the same as the present limitation. Please see the discussion under the **CLAIM 74, *Limitation [2]*** heading which includes an *In Re Donaldson Co.* analysis of the limitation.

Limitation [3]

Carroll et al. does not disclose transponder 40's modulating the alternating field generated by transponder 40 with a sequence of bits to be communicated to controller 10 whereby the start of

each transmitted bit is governed by a bit-timing clock signal that is synchronized to a bit-timing clock signal embedded by controller 10 in the alternating magnetic field generated by controller 10. A bit-timing clock signal that is synchronized to a bit-timing clock signal embedded by controller 10 in the alternating magnetic field generated by controller 10 is simply not available in transponder 40 (see ***Limitations [1] and [2]***).

Carroll et al. does not describe each and every element of claim 75 and therefore did not anticipate applicants' claim-75 invention.

CLAIM 76

Claim 76 reads as follows:

76. A method of communication between an interrogator and a responder, the method performed by the interrogator comprising the steps:

generating an alternating magnetic field;

[1] embedding a bit-timing clock signal in the alternating magnetic field;

extracting data communicated by the responder from an alternating magnetic field generated by the responder;

the method performed by the responder comprising the steps:

[2] extracting the bit-timing clock signal from the alternating magnetic field generated by the interrogator;

[3] generating a bit-timing clock signal that is synchronized to the bit-timing clock signal originating with the interrogator;

generating an alternating magnetic field;

[4] embedding data to be communicated to the interrogator in the alternating magnetic field generated by the responder, the start of each bit being controlled by the bit-timing clock signal generated by the responder.

Carroll et al. does not disclose any of Limitations [1], [2], [3], and [4].

Limitation [1]

Carroll et al. does not disclose "embedding a bit-timing clock signal in the alternating magnetic field", a limitation also present in claim 70. For arguments in support of this assertion, please see the discussion above under the ***Claim 70*** heading.

Limitation [2]

Since Carroll et al. does not disclose "embedding a bit-timing clock signal in the alternating magnetic field", it follows that Carroll et al. could not (and does not) disclose "extracting the bit-timing clock signal from the alternating magnetic field generated by the interrogator". The only extraction performed by Carroll et al.'s transponder 40 is the extraction of data from the incoming FSK modulated signal from controller 10 (col. 12, lines 20-34), the FSK modulated signal being produced by shifting the frequency of the signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a data pulse. Carroll et al., col. 7, lines 16-29.

Extracting the data from an FSK modulated signal is NOT the same as extracting a bit-timing clock signal.

The examiner argues that "[e]lements 58 and 60 extract the bit timing clock signal from the carrier generated by the interrogator." 01/15/04 Office Action, p. 17. Element 58 amplifies the 125-kHz carrier transmitted by controller 10, and element 60 divides the 125-kHz carrier by 64 to obtain a clock signal having a frequency equal to the bit rate (Fig. 3, divide-by-64 timing control 60). But generating a clock signal having the a frequency equal to the bit rate by dividing down the frequency of the carrier signal is not the same as "EXTRACTING a bit-timing clock signal that is embedded in the carrier signal. The dictionary definition of "extract" is "to pull or draw out". *The Random House College Dictionary, Revised Edition*, Random House, Inc. 1988. "Pulling or drawing out the bit-timing clock signal from the alternating magnetic field generated by the interrogator" implies that there is a unique bit-timing clock signal contained in the alternating magnetic field which can be pulled out. The clock signal that one obtains by dividing down the carrier signal is not unique. There are 64 possible clock signals that could be obtained, depending on when the divide-by-64 timing control begins to count. There is no reasonable interpretation of the language of limitation [2] that would allow one to conclude that a synchronous counter is a disclosure of the limitation.

As a result of a Federal Circuit decision, examiners are required to interpret a step-plus-function limitation in a claim in terms of the corresponding structure, materials or acts described in the specification:

> **"As a consequence of a decision by the Court of Appeals for the Federal Circuit in its en banc decision In re Donaldson Co., 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994), "examiners must interpret a 35 U.S.C. 112, sixth paragraph 'means or step plus function' limitation in a claim as limited to the corresponding structure, materials or acts described in the specification and equivalents thereof. . . ." MPEP § 2181.**

The limitation "***extracting the bit-timing clock signal from the alternating magnetic field generated by the interrogator***" should be considered to be a step-plus-function element since "the

element at issue sets forth a step for reaching a particular result, but not the specific technique or procedure used to achieve the result." *Caterpillar Inc. v. Detroit Diesel Corp.*, 41 USPQ2d 1876, 1882 (N.D. Ind. 1996) (cited in MPEP § 2181). Thus, this limitation is subject to the requirements of *In re Donaldson Co.*

"Extracting the bit-timing clock signal from the alternating magnetic field generated by the interrogator" is accomplished as described in paragraphs 0111 through 0115 of the Specification using the devices identified in these paragraphs and shown in Fig. 18. The devices in Carroll et al. identified by the examiner as performing this function are amplifier 58 and a ten-bit synchronous counter 60. These two devices are not the equivalent of the circuitry identified in paragraphs 0111 through 0115 of the Specification and shown in Fig. 18.

An *In re Donaldson Co.* analysis comes to the same conclusion as a straightforward analysis of the words of the claim. Carroll et al. does not disclose appellants' circuitry for "extracting the bit-timing clock signal from the alternating magnetic field generated by the interrogator", or equivalents thereof, and consequently did not anticipate limitation [2] of appellants' claim-76 invention.

Limitation [3]

Carroll et al. does not disclose "generating a bit-timing clock signal that is synchronized to the bit-timing clock signal originating with the interrogator".

Carroll et al. discloses the generation of a clock signal having a frequency equal to the bit rate (see *Limitation [2]*). However, Carroll et al. does not disclose any operations that suggest synchronizing this clock signal with any other clock signal having a frequency equal to the bit rate let alone a clock signal having a frequency equal to the bit rate and originating with controller 10.

The examiner argues that "[t]he sync generator 70 is synchronized to the received clock signal since the timing control element 60 drives all the elements that follow, etc 64,48,68 and 70." 08/12/03 Office Action, p. 19. The "received clock signal" which the examiner refers to is the carrier transmitted by controller 10. It is not the bit-timing clock signal embedded in the carrier that is specified in limitation [3].

As a result of a Federal Circuit decision, examiners are required to interpret a step-plus-function limitation in a claim in terms of the corresponding structure, materials or acts described in the specification:

> **"As a consequence of a decision by the Court of Appeals for the Federal Circuit in its en banc decision In re Donaldson Co., 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994), "examiners must interpret a 35 U.S.C. 112, sixth paragraph 'means or step plus function' limitation in a claim as limited to the corresponding structure, materials or acts described in the specification and equivalents thereof . . . ." MPEP § 2181.**

The limitation "*generating a bit-timing clock signal that is synchronized to the bit-timing clock signal originating with the interrogator*" should be considered to be a step-plus-function element since "the element at issue sets forth a step for reaching a particular result, but not the specific technique or procedure used to achieve the result." *Caterpillar Inc. v. Detroit Diesel Corp.*, 41 USPQ2d 1876, 1882 (N.D. Ind. 1996) (cited in MPEP § 2181). Thus, this limitation is subject to the requirements of *In re Donaldson Co.*

"Generating a bit-timing clock signal" is accomplished as described in paragraph 0117 of the Specification. "Generating a bit-timing clock signal that is synchronized to the bit-timing clock signal originating with the interrogator" is accomplished as described in paragraphs 0111 through 0119 of the Specification using the devices identified in these paragraphs and shown in Fig. 18. The devices in Carroll et al. identified by the examiner as performing this function are amplifier 58 and

a ten-bit synchronous counter 60. These two devices are not the equivalent of the circuitry identified in paragraphs 0111 through 0115 of the Specification and shown in Fig. 18.

An *In re Donaldson Co.* analysis comes to the same conclusion as a straightforward analysis of the words of the claim. Carroll et al. does not disclose appellants' circuitry for "generating a bit-timing clock signal that is synchronized to the bit-timing clock signal originating with the interrogator", or equivalents thereof, and consequently did not anticipate Limitation [3] of appellants' claim-76 invention.

Limitation [4]

Carroll et al. does not disclose "***embedding data to be communicated to the interrogator in the alternating magnetic field generated by the responder, the start of each bit being controlled by the bit-timing clock signal generated by the responder***". Carroll et al. does not disclose transponder 40's embedding data to be communicated to controller 10 in the alternating magnetic field generated by transponder 40 whereby the start of each bit is controlled by a bit-timing clock signal that is synchronized to the bit-timing clock signal originating with controller 10. A bit-timing clock signal that is synchronized to a bit-timing clock signal embedded by controller 10 in the alternating magnetic field generated by controller 10 is simply not available in transponder 40 (see discussion under the ***Limitation [3]*** heading).

Carroll et al. does not describe each and every element of claim 76 and therefore did not anticipate appellants' claim-76 invention.

CLAIM 77

Claim 77 reads as follows:

77. A method of communication between an interrogator and a responder, the method performed by the interrogator comprising the steps:

generating an alternating magnetic field;

[1] embedding a bit-timing clock signal in the alternating magnetic field;

embedding data to be communicated to the responder in the alternating magnetic field;

the method performed by the responder comprising the steps:

[2] extracting a bit-timing clock signal from the alternating magnetic field generated by the interrogator;

[3] performing at least one weighted integration of a signal derived from the alternating magnetic field generated by the interrogator over a bit period using the bit-timing clock signal to identify the beginning and end of a bit period;

[4] identifying the bit being transmitted during each bit period utilizing the weighted integration(s).

Carroll et al. does not disclose any of limitations [1], [2], [3], and [4].

Limitation [1]

Carroll et al. does not disclose "embedding a bit-timing clock signal in the alternating magnetic field", **a limitation also present in claim 70. For arguments in support of this assertion, please see the discussion above under the CLAIM 70 heading.**

Limitation [2]

Carroll et al. does not disclose "extracting the bit-timing clock signal from the alternating magnetic field generated by the interrogator", a limitation also present in claim 76. For arguments in support of this assertion, please see the discussion above under the **CLAIM 76,** ***Limitation [2]*** headings.

Limitation [3]

Carroll et al. does not disclose "performing at least one weighted integration of a signal derived from the alternating magnetic field generated by the interrogator over a bit period using the bit-timing clock signal to identify the beginning and end of a bit period", a limitation also present in claim 74. For arguments in support of this assertion, please see the discussion above under the **CLAIM 74,** ***Limitation [3]*** heading.

Limitation [4]

Carroll et al. does not disclose "identifying the bit being transmitted during each bit period utilizing the weighted integration(s)", a limitation also present in claim 74. For arguments in support of this assertion, please see the discussion above under the **CLAIM 74,** ***Limitation [4]*** heading.

Carroll et al. does not describe each and every element of claim 77 and therefore did not anticipate applicants' claim-77 invention.

CLAIM 78

Claim 78 reads as follows:

78. An apparatus for practicing the method of claim 73.

Carroll et al. did not anticipate claim 73 and consequently did not anticipate claim 78 which depends from claim 73.

The examiner responded to the above argument as follows:

"Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references." 01/15/04 Office Action, pp. 18-19.

Appellants' have pointed out how the language of claim 73 (see discussion under the CLAIM 73 heading), from which claim 78 depends, distinguishes it from the references.

CLAIM 79

Claim 79 reads as follows:

79. An apparatus for practicing the method of claim 76.

Carroll et al. did not anticipate claim 76 and consequently did not anticipate claim 79 which depends from claim 76.

The examiner responded to the above argument as follows:

"Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references." 01/15/04 Office Action, pp. 18-19.

Appellants' have pointed out how the language of claim 76 (see discussion under the CLAIM 76 heading), from which claim 79 depends, distinguishes it from the references.

CLAIM 80

Claim 80 reads as follows:

80. An apparatus for practicing the method of claim 77.

Carroll et al. did not anticipate claim 77 and consequently did not anticipate claim 80 which depends from claim 77.

The examiner responded to the above argument as follows:

"Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references." 01/15/04 Office Action, pp. 18-19.

Appellants' have pointed out how the language of claim 77 (see discussion under the CLAIM 77 heading), from which claim 80 depends, distinguishes it from the references.

V. WHETHER CLAIMS 1, 3, 41, AND 43 ARE UNPATENTABLE UNDER 35 U.S.C. § 103(A) IN VIEW OF CHATELOT (U.S. 4,864,633) AND KURUSU (U.S. 3,587,017).

CLAIM 1

Claim 1 reads as follows:

1. A reader for use with a tag that communicates data to the reader, the reader comprising:

[1] a transformer having a plurality of windings, each winding having first and second terminals;

a coil driver having first and second output terminals;

[2] two capacitors, each capacitor having first and second terminals, the first and second output terminals of the coil driver being connected to the first terminals of the capacitors, the second terminals of the capacitors being connected to the first and second terminals of a winding of the transformer;

[3] a coil having first and second terminals connected respectively to the first and second end terminals of a winding of the transformer;

[4] a data extractor for extracting data from the signal induced in the coil, the data extractor having first and second terminals connected respectively to first and second terminals of a winding of the transformer.

Neither Chatelot nor Kurusu disclose the limitations in boldface.

To establish a *prima facie* case of obviousness, three basic criteria must be satisfied:

"To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)." MPEP § 2142.

Limitation [1]

Chatelot does not disclose the use of a transformer by a reader in communicating with a tag. The transmission circuit 21 connects to coil 13 only through capacitors as does the reception circuit 22. Chatelot, Fig. 3.

Kurusu discloses a transformer as an impedance matching device between a filter and an amplifier in an overvoltage-protecting arrangement. Kurusu's application does not envision the use of a single transformer in both transmitting and receiving signals as specified by Limitations [2], [3], and [4]. Thus, neither Chatelot nor Kurusu disclose a multi-purpose transformer as specified in claim 1.

Limitation [2]

As the examiner has pointed out, Chatelot does not disclose Limitation [2]. 01/15/04 Office Action, p. 4.

Kurusu shows a receiving antenna 11 that feeds a received signal through a filter 13 to amplifier 12 which outputs an amplified version of the received signal. Amplifier 12 includes input coupling transformer 17, capacitor 22 connected across the input winding of transformer 17, and RC

circuit 21 which (together with RC circuit 23) provides proper biasing of transistor 16. Kurusu, Fig. 1.

The examiner argues that Chatelot's capacitors 19 are analogous to Kurusu's capacitor in RC circuit 21 and Chatelot's transmission coil 13 is analogous to Kurusu's receiving antenna 11. *See* Chatelot, Fig. 3. The examiner then concludes that it would be obvious to one skilled in the art to combine Kurusu's transformer 17 with Chatelot's capacitors 19 and transmission coil 13 and thereby achieve applicants' claim-1 invention. 01/15/04 Office Action, pp 4-5.

With respect to teaching or suggesting limitation [2], there is no teaching or suggestion of "two capacitors, each capacitor having first and second terminals, the first and second output terminals of the coil driver being connected to the first terminals of the capacitors, the second terminals of the capacitors being connected to the first and second terminals of a winding of the transformer". The capacitor in RC circuit 21 (Kurusu, Fig. 1) is connected to ground rather than being analogous to Chatelot's capacitors 19 which provide passageways for driving signals to coil 13. Thus, Kurusu provides no information as to how to incorporate Kurusu's transformer in Chatelot's invention. Does the person skilled in the art simply insert Kurusu's transformer 17 between Chatelot's capacitors 19 and coil 13 as applicants specify in claim 1? Or does the person skilled in the art place Kurusu's transformer 17 on the other side of Chatelot's capacitors 19? There is no teaching as to what to do.

The examiner responded to the arguments presented in the above paragraph by providing a hand-drawn drawing showing a transformer coupling capacitors to an antenna coil which seems to be based on appellants' Fig. 1 with the coupling circuit 7 replaced by appellants' transformer of either

Fig. 3 or 4. 01/15/04 Office Action, p.5. Appellants' Specification and drawings are not a proper source of disclosure in support of an obviousness rejection.

> **Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)." MPEP § 2142.**

Neither Chatelot nor Kurusu disclose appellants' limitation [2].

Limitation [3]

Chatelot does not disclose the use of a transformer in coupling coil 13 to either transmission circuit 21 or reception circuit 22. Chatelot, Fig. 3. The only connections to coil 13 are through capacitors 19. Chatelot, Fig. 2.

Kurusu discloses the two terminals of antenna 11 connected to the two input terminals of filter 13. Neither Chatelot nor Kurusu disclose "a coil having first and second terminals connected respectively to the first and second end terminals of a winding of the transformer."

Limitation [4]

Limitation [4] specifies "a data extractor having first and second terminals connected respectively to first and second terminals of a winding of the transformer."

Chatelot does not disclose this limitation since Chatelot does not disclose a transformer located between capacitor(s) 19 and coil 13. Chatelot extracts data from signals picked up from the capacitor terminals NOT connected to the coil (Chatelot, Fig. 3), and consequently, even if Chatelot

had disclosed a transformer located between capacitor(s) 19 and coil 13, he would not have disclosed limitation [4].

Kurusu discloses an amplifier connected to a winding of transformer 17, but transformer 17 is not the multiple-purpose transformer called for by Limitations [2], [3], and [4].

There is no teaching in Chatelot and/or Kurusu that would cause a person skilled in the art to incorporate the transformer disclosed by Kurusu in Chatelot's invention at a location between capacitor(s) 19 and coil 13.

Motivation

With respect to motivation, there is nothing in Chatelot that suggests the substitution of a transformer for the direct connections of capacitors 19 to coil 13. There is nothing in the category of "knowledge generally available to one of ordinary skill in the art" that suggests this substitution.

Nor would a person skilled in the art be motivated to substitute a transformer employed in an overvoltage protecting arrangement for an RF amplifier used to amplify received signals. Kurusu, col. 1, lines 5-73. The use of a transformer for coupling received signals into an amplifier (Kurusu) has little or nothing to do with coupling a driving signal to a coil (Chatelot).

The examiner responds to these arguments by arguing that the general knowledge that a transformer coupling provides isolation between circuits is sufficient motivation. 08/12/03 Office Action, p. 21. The examiner did not explain why isolation between circuits is needed or even desirable in the Chatelot invention.

In his 01/15/04 Office Action, p. 19, the examiner qualified his assertion that "the general knowledge that a transformer coupling provides isolation between circuits is sufficient motivation"

by adding the words "UNLESS THE APPLICANT CAN PROVE THAT SUCH FUNCTION WOULD NOT BE DESIRABLE."

The examiner has it backwards. It is not up to the applicant to prove the undesirability of transformer coupling. It is up to the examiner to provide a convincing line of reasoning as to the desirability of transformer coupling. *Ex parte Clapp*, 227 USPQ 972, 973 (Bd Pat. App. & Inter. (1985) (cited in MPEP § 2142).

Chatelot and Kurusu in combination fail to teach all of the claim limitations of claim 1. Even if the combination did teach all of the claim limitations of claim 1, there is no motivation for a person skilled in the art to make such a combination. The examiner did not establish the *prima facie* obviousness of claim 1.

CLAIM 3

Claim 3 reads as follows:

3. The reader of claim 1 wherein the transformer has a first winding and a second winding, the capacitors being connected to the first winding, the coil being connected to the second winding, and the data extractor being connected to the second winding.

Neither Chatelot nor Kurusu show the configuration specified in claim 3. Nor would a person skilled in the art be motivated to modify Chatelot's invention in conformance with applicants' claim-3 limitations. Specifically, neither Chatelot nor Kurusu disclose a transformer coupling a coil

through capacitors to a coil driver wherein a data extractor is connected to the same transformer winding as the coil. For details, please see discussion above under the **CLAIM 1** heading.

The examiner has not established the *prima facie* obviousness of claim 3.

CLAIM 41

Claim 41 reads as follows:

41. A tag for use with a reader, the tag comprising:

[1] a transformer having a plurality of windings, each winding having first and second terminals;

[2] a coil having first and second terminals connected respectively to the first and second terminals of a winding of the transformer;

[3] a capacitor having first and second terminals connected respectively to the first and second terminals of a winding of the transformer;

[4] a coil driver having first and second terminals connected respectively to the first and second terminals of a winding of the transformer;

[5] a data extractor for extracting data from the signal induced in the coil, the data extractor having first and second terminals connected to the first and second terminals of a winding of the transformer;

[6] a power extractor for extracting power from the signal induced in the coil to operate the tag, the power extractor having first and second terminals connected respectively to the first and second terminals of a winding of the transformer.

Neither Chatelot nor Kurusu, separately or in combination, disclose the limitations shown in boldface.

Chatelot discloses data carrier 12 as having transmission-reception coil 14, transmission and reception circuits to be coupled to a resonant circuit to which coil 14 belongs, logic interposed between the transmission and reception circuits, and a data memory or other digital supply. No structural details are provided. Chatelot, col. 2, lines 45-61. With no structural details for data carrier available 12 available, the examiner resorts to the structural details pertaining to Chatelot's reading-writing station 11 (the counterpart of appellants' reader) as the foundation for the rejection of claim 41 for a tag. 01/15/04 Office Action, p. 5.

Limitation [1]

Chatelot does not disclose the use of a transformer by either transmission circuit 11 or data carrier 12 in communicating with one another.

Kurusu discloses a transformer as an impedance matching device between a filter and an amplifier in an overvoltage-protecting arrangement for an RF amplifier. Kurusu's application does not envision the use of a single transformer in both transmitting and receiving signals and in power extraction as specified by limitations [2], [3], [4], [5], and [6].

Thus, neither Chatelot nor Kurusu disclose a multi-purpose transformer as specified in claim 41.

The examiner argues that "Kurusu shows a transformer connecting a capacitor 21 and other circuits to the antenna 11" (01/15/04 Office Action, p. 5), suggesting that Kurusu's transformer is a

multipurpose coupling device, but this statement is incorrect. Kurusu's transformer 17 is a single-purpose transformer which provides input coupling to RF amplifier 12.

The examiner supposedly demonstrates how the combination of the Chatelot and Kurusu inventions results in appellants' claim-41 invention by showing Kurusu's transformer inserted into a simplified schematic of the transmission portion of Chatelot's reading-writing station 11. 01/15/04 Office Action, p. 5. But the combination of Chatelot and Kurusu that the examiner proposes does not in accordance with any of the limitations [2] through [6]. Moreover, there is nothing in Kurusu that suggests that a transformer be used as a multipurpose coupling device.

Limitation [2]

The two terminals of Kurusu's antenna 11 (corresponding to applicants' coil) connects to the two terminals of filter 13. Thus, neither Chatelot nor Kurusu discloses "a coil having first and second terminals connected respectively to the first and second terminals of a winding of the transformer." In fact, Kurusu's transformer 17 presumably cannot interface the RF amplifier 12 directly with antenna 11 because the filter 11 is required to match the impedance of the antenna to transistor 16. Kurusu, col. 1, lines 35-37.

Limitation [3]

The first terminals of Chatelot's capacitors 19 connect to the first and second terminals of Chatelot's transmission circuit 21 (applicants' driver). The second terminals of Chatelot's capacitors 19 connect to the first and second terminals of Chatelot's coil 13. Only one terminal of Kurusu's capacitor 21 connects to transformer winding 19. Thus, neither Chatelot nor Kurusu disclose "a

capacitor having first and second terminals connected respectively to the first and second terminals of a winding of the transformer."

The examiner argues that Chatelot's capacitors 19 are analogous to Kurusu's capacitor in RC circuit 21 and Chatelot's transmission coil 13 is analogous to Kurusu's receiving antenna 11. *See* Chatelot, Fig. 3. The examiner then concludes that it would be obvious to one skilled in the art to combine Kurusu's transformer 17 with Chatelot's capacitors 19 and transmission coil 13 and thereby achieve applicants' claim-41 invention. 01/15/04 Office Action, pp 4-5.

Since the first terminal of Kurusu's capacitor in RC circuit 21 is connected to a first terminal of winding 18 of transformer 17 and the second terminal of Kurusu's capacitor is connected to a first terminal of winding 19 of transformer 17, this arrangement with Chatelot's capacitors 19 taking the place of Kurusu's capacitor does not result in the arrangement specified by the limitation "a capacitor having first and second terminals connected respectively to the first and second terminals of a winding of the transformer."

Limitation [4]

Chatelot does not disclose how the driver is connected to the coil driver in data carrier 12 (analogous to appellants' tag). In Chatelot's reading-writing station 11 (analogous to appellants' reader), transmission circuit 21 connects to coil 13 through capacitors 19. Thus, Chatelot does not disclose limitation [4].

Kurusu does not disclose a driver and provides no insight as to how a driver would be incorporated in his invention of an overvoltage protecting arrangement for an RF amplifier. The

examiner does suggest how the Kurusu and Chatelot inventions could be combined to achieve limitation [4] when neither one separately discloses the limitation. 01/15/04 Office Action, p. 5.

There is no basis for arguing that Chatelot and Kurusu can be combined in a way that will result in the limitation "a driver having first and second terminals connected respectively to the first and second terminals of a winding of the transformer."

Limitation [5]

Chatelot does not disclose how a data extractor is connected to the coil in data carrier 12 (analogous to appellants' tag). In Chatelot's reading-writing station 11 (analogous to appellants' reader), reception circuit 22 connects to coil 13 through capacitors 19. Thus, Chatelot does not disclose limitation [5].

The input terminals to Kurusu's transistor 16 (corresponding to the input of a "data extractor") connect to the series combination of winding 19 of transformer 17 and the RC circuit 21. This connection arrangement is not the one specified in the limitation "a data extractor for extracting data from the signal induced in the coil, the data extractor having first and second terminals connected to the first and second terminals of a winding of the transformer."

Limitation [6]

And finally, neither Chatelot nor Kurusu disclose circuitry, either separately or in combination, which would correspond to the limitation "a power extractor for extracting power from the signal induced in the coil to operate the tag, the power extractor having first and second terminals connected respectively to the first and second terminals of a winding of the transformer."

The examiner's only response to the above arguments was as follows:

"Regarding the 103 rejections of claim 41 (Chatelot and Kurusu or Ogita). The applicants argue that Chatelot does not show the limitations of element 1. This appears to be the only argument for this claim (with this rejection). One cannot show nonobviousness by attacking references individually where the rejections are abased on combinations of references." 01/15/04 Office Action, p. 20.

Neither Chatelot nor Kurusu disclose the limitations specified in claim 41. Neither Chatelot nor Kurusu provide motivation to a person skilled in the art to attempt a combination of Chatelot and Kurusu that would result in applicants' claim-41 invention.

The examiner states that "it would be obvious to one of ordinary skill in the art at the time of the invention to have used a transformer in the Chatelot system to provide isolation between the communication antenna coil and the other circuits in the reader as suggested by Kurusu." 01/15/04 Office Action, p. 5. Kurusu does not suggest using a transformer to provide isolation. Kurusu's transformer is simply a convenient way of coupling the output of filter 13 to transistor 16. Kurusu, col. 2, lines 36-47. Moreover, simply stating a possible reason for incorporating a transformer in Chatelot's invention is not sufficient to establish motivation:

> **"To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references."** *Ex parte Clapp*, 227 USPQ 972, 973 (Bd Pat. App. & Inter. 1985) (cited in MPEP § 2142).

The examiner has not established the *prima facie* obviousness of claim 41.

CLAIM 43

Claim 43 reads as follows:

43. The tag of claim 41 wherein the transformer has a first winding and a second winding, the capacitor and the driver being connected to the first winding, the coil, the data extractor, and the power extractor being connected to the second winding.

Chatelot discloses data carrier 12 as having transmission-reception coil 14, transmission and reception circuits to be coupled to a resonant circuit to which coil 14 belongs, logic interposed between the transmission and reception circuits, and a data memory or other digital supply. No structural details are provided. Chatelot, col. 2, lines 45-61. With no structural details for data carrier available 12 available, the examiner resorts to the structural details pertaining to Chatelot's reading-writing station 11 (the counterpart of appellants' reader) as the foundation for the rejection of claim 43 for a tag. 01/15/04 Office Action, p. 5.

Neither Chatelot nor Kurusu disclose "the capacitor and the driver being connected to the first winding" nor do they disclose "the coil, the data extractor, and the power extractor being connected to the second winding."

The references also do not provide any motivation to a person skilled in the art to incorporate a transformer in Chatelot's invention for the purpose of achieving an invention with the limitations of claim 43.

The examiner did not address the specific limitations of claim 43 in either the 08/12/03 Office Action or the 01/15/04 Office Action. Nor did he refute the argument given above in the 01/15/04 Office Action. Instead, he commented as follows:

> "Regarding the 103 rejections of claim 42-45 (Chatelot and Kurusu or Ogita). Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references." 01/15/04 Office Action, p. 20.

Appellants' argument states very clearly that a transformer which interconnects a capacitor, a driver, a coil, a data extractor, and a power extractor as prescribed in the claim is not disclosed by either of the references. What more can be said without more meaningful responses from the examiner?

The examiner states that "it would be obvious to one of ordinary skill in the art at the time of the invention to have used a transformer in the Chatelot system to provide isolation between the communication antenna coil and the other circuits in the reader as suggested by Kurusu." 01/15/04 Office Action, p. 5.

Kurusu does not suggest using a transformer to provide isolation. Kurusu's transformer is simply a convenient way of coupling the output of filter 13 to transistor 16. Kurusu, col. 2, lines 36-47. Moreover, simply stating a possible reason for incorporating a transformer in Chatelot's invention is not sufficient to establish motivation:

> **"To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings**

of the references." *Ex parte Clapp*, 227 USPQ 972, 973 (Bd Pat. App. & Inter. 1985) (cited in MPEP § 2142).

The examiner has not established the *prima facie* obviousness of claim 43.

VI. WHETHER CLAIMS 1, 2, 4, 41, 42, 44, AND 45 ARE UNPATENTABLE UNPATENTABLE UNDER 35 U.S.C. § 103(A) IN VIEW OF CHATELOT (U.S. 4,864,633) AND OGITA ET AL. (U.S. 4,278,980).

CLAIM 1

Claim 1 reads as follows:

1. A reader for use with a tag that communicates data to the reader, the reader comprising:

[1] a transformer having a plurality of windings, each winding having first and second terminals;

a coil driver having first and second output terminals;

[2] two capacitors, each capacitor having first and second terminals, the first and second output terminals of the coil driver being connected to the first terminals of the capacitors, the second terminals of the capacitors being connected to the first and second terminals of a winding of the transformer;

[3] a coil having first and second terminals connected respectively to the first and second end terminals of a winding of the transformer;

[4] a data extractor for extracting data from the signal induced in the coil, the data extractor having first and second terminals connected respectively to first and second terminals of a winding of the transformer.

Neither Chatelot nor Ogita et al. nor the references in combination disclose any of the limitations in boldface.

Limitation [1]

Although limitation [1] does not specifically state that the transformer is a multipurpose device, it clearly is, as indicated by limitations [2], [3], and [4]. It is obviously an important consideration in the design of the transformer that is the subject of limitation [1].

Chatelot does not disclose even a single-purpose use of a transformer by a reader in communicating with a tag. Ogita et al. discloses a transformer as an impedance matching device between a coil and an amplifier. Ogita et al., Fig. 8. Ogita et al.'s application does not envision the use of a single transformer in both transmitting and receiving signals as specified by limitations [2], [3], and [4].

Thus, neither Chatelot nor Ogita et al. disclose the transformer specified in claim 1 which can meet the multipurpose use specified in limitations [2], [3], and [4].

Limitation [2]

Chatelot discloses a transmission circuit 21 driving coil 13 through capacitors 19 connected directly to coil 13. Chatelot, Figs. 2 and 3. Thus, Chatelot discloses the first part of Limitation [2], "two capacitors, each capacitor having first and second terminals, the first and second output terminals of the coil driver being connected to the first terminals of the capacitors." Chatelot does not disclose the second part of Limitation [2], "the second terminals of the capacitors being connected to the first and second terminals of a winding of the transformer."

Ogita et al. shows a receiving antenna 21 that feeds a received signal through impedance-matching transformer 31 to amplifier 37. Ogita et al., Fig. 8. Ogita et al.'s capacitor 34 is merely a tuning capacitor (Ogita et al., col. 6, lines 7-11) and not the analog of Chatelot's coupling capacitors

19 which are the pathways between Chatelot's transmission circuit 21 and reception circuit 22 to coil 13..

Ojita et al.'s teaching of the use of a transformer for matching impedances in a receiving circuit is not a teaching of the use of a transformer in Chatelot's transmission circuit for coupling capacitors 19 to coil 13 so that transmission circuit 21 can send driving signals through capacitors 19 to coil 13.

Limitation [3]

Chatelot does not disclose the use of a transformer in communicating with data carrier 12. Chatelot, Figs. 2 and 3.

Ogita et al. discloses the two terminals of loop antenna 21 connected to an end terminal and a tap terminal (NOT the two end terminals) of winding 32 of transformer 31. Neither Chatelot nor Ogita et al. disclose "a coil having first and second terminals connected respectively to the first and second end terminals of a winding of the transformer."

Limitation [4]

Limitation [4] specifies "a data extractor having first and second terminals connected respectively to first and second terminals of a winding of the transformer."

Chatelot does not disclose this limitation since Chatelot does not disclose a transformer located between capacitor(s) 19 and coil 13. Chatelot extracts data from signals picked up from the capacitor terminals NOT connected to the coil (Chatelot, Fig. 3), and consequently, even if Chatelot

had disclosed a transformer located between capacitor(s) 19 and coil 13, he would not have disclosed limitation [4].

Ogita et al. shows a receiving antenna 21 that feeds a received signal through impedance-matching transformer 31 to amplifier 37. Ogita et al., Fig. 8. Ogita et al.'s capacitor 34 is merely a tuning capacitor (Ogita et al., col. 6, lines 7-11) and not the analog of Chatelot's capacitors 19.

Ogita et al. discloses amplifier 37 connected to winding 33 of transformer 31, but transformer 31 is not the multiple-purpose transformer called for by Limitations [2], [3], and [4].

There is no teaching in Chatelot and/or Ogita et al. that would motivate a person skilled in the art to incorporate the transformer disclosed by Ogita et al. in Chatelot's invention at a location between capacitor(s) 19 and coil 13.

The examiner concludes that it would be obvious to one skilled in the art to combine Ogita et al.'s transformer 31 with Chatelot's capacitors 19 and transmission coil 13 and thereby achieve applicants' claim-1 invention. 01/15/04 Office Action, p. 6. The problem with the examiner's conclusion is that it is not clear how this combination would be accomplished.

Capacitor 34 (Ogita et al., Fig. 8) is connected to ground rather than being analogous to Chatelot's capacitors 19 which provide passageways for driving signals to coil 13. Thus, Ogita et al. provides no information as to how to incorporate Ogita et al.'s transformer in Chatelot's invention. Does the person skilled in the art simply insert Ogita et al.'s transformer 31 between Chatelot's capacitors 19 and coil 13 as appellants specify in claim 1? Or does the person skilled in the art place Ogita et al.'s transformer 31 on the other side of Chatelot's capacitors 19? There is no teaching in either of the references as to what to do.

With respect to motivation, there is nothing in Chatelot that suggests the substitution of a transformer for the direct connections of capacitors 19 to coil 13. There is nothing in the category of "knowledge generally available to one of ordinary skill in the art" that suggests this substitution.

Nor would a person skilled in the art be motivated to substitute a transformer employed in impedance-matching a receiving antenna to an amplifier for Chatelot's direct connections of capacitors 19 to coil 13. The use of a transformer for impedance matching in a receiving circuit (Ogita et al.) has little or nothing to do with coupling a driving signal to a coil for the purpose of interrogating a tag (Chatelot).

Nor would a person skilled in the art be motivated to use Ogita et al.'s transformer for coupling the data extractor to the coil as specified in Limitation [4]. Ogita et al. discloses nothing concerning the use of a common capacitor-coil configuration, where the coil and capacitor(s) are coupled together by a transformer means, for both transmitting and receiving signals.

The examiner argues that the motivation for incorporating Ogita et al.'s transformer in Chatelot's invention is "to provide isolation between the communication antenna coil and the other circuits in the reader." 01/15/04 Office Action, p. 6. However, such a modification would appear to be unnecessary since Chatelot states that with his reading-writing station "a rapid and reliable data exchange may be made with a user system such as a programmable automation or other system controlling an industrial process." Chatelot, col. 2, lines 3-6. Where is the motivation to modify (and at the same time complicate) a system that is already capable of operating satisfactorily? Furthermore, Ogita et al. teaches the use of a transformer for impedance matching—not for providing isolation between the communication antenna coil and the other circuits in the reader.

The examiner responds to these arguments by arguing that the general knowledge that a transformer coupling provides isolation between circuits is sufficient motivation. 08/12/03 Office Action, p. 21. The examiner did not explain why isolation between circuits is needed or even desirable in the Chatelot invention.

In his 01/15/04 Office Action, p. 19, the examiner qualified his assertion that the "general knowledge that a transformer coupling provides isolation between circuits" is sufficient motivation by adding the words "UNLESS THE APPLICANT CAN PROVE THAT SUCH FUNCTION WOULD NOT BE DESIRABLE."

The examiner's approach to establishing motivation is novel and incorrect. It is not up to the applicant to prove the undesirability of transformer coupling. It is up to the examiner to provide a convincing line of reasoning as to the desirability of transformer coupling. *Ex parte Clapp*, 227 USPQ 972, 973 (Bd Pat. App. & Inter. (1985) (cited in MPEP § 2142).

Chatelot and Ogita et al. in combination fail to teach all of the claim limitations of claim 1. Even if the references did teach all of the claim limitations of claim 1, there is no motivation for a person skilled in the art to make such a combination.

The examiner has not established the *prima facie* obviousness of claim 1.

CLAIM 2

Claim 2 reads as follows:

2. *The reader of claim 1 wherein the transformer has a first winding and a second winding, the capacitors being connected to the first winding, the coil being connected to the second winding, and the data extractor being connected to the first winding.*

Neither Chatelot nor Ogita et al. disclose the configuration specified in claim 2. Specifically, neither Chatelot nor Ogita et al. disclose a transformer coupling a coil through capacitors to a coil driver wherein a data extractor is connected to the same transformer winding as the capacitors. Nor is any motivation provided in either reference that would cause a person skilled in the art to modify Chatelot's invention in conformance with applicants' claim-2 limitations. For details, please see discussion above under the **CLAIM 1** heading.

The examiner has not established the *prima facie* obviousness of claim 2.

CLAIM 4

Claim 4 reads as follows:

4. The reader of claim 1 wherein the transformer has a first winding, a second winding, and a third winding, the capacitors being connected to the first winding, the coil being connected to the second winding, and the data extractor being connected to the third winding.

Neither Chatelot nor Ogita et al. disclose the configuration specified in claim 4. Specifically, neither Chatelot nor Ogita et al. disclose a transformer coupling a coil through capacitors to a coil driver by means of two transformer windings and a data extractor connected to a third transformer winding. Nor would a person skilled in the art be motivated to modify Chatelot's invention in conformance with applicants' claim-4 limitations. For details, please see discussion above under the **CLAIM 1** heading.

The examiner has not established the *prima facie* obviousness of claim 4.

CLAIM 41

Claim 41 reads as follows:

41. A tag for use with a reader, the tag comprising:

[1] a transformer having a plurality of windings, each winding having first and second terminals;

[2] a coil having first and second terminals connected respectively to the first and second terminals of a winding of the transformer;

[3] a capacitor having first and second terminals connected respectively to the first and second terminals of a winding of the transformer;

[4] a coil driver having first and second terminals connected respectively to the first and second terminals of a winding of the transformer;

[5] a data extractor for extracting data from the signal induced in the coil, the data extractor having first and second terminals connected to the first and second terminals of a winding of the transformer;

[6] a power extractor for extracting power from the signal induced in the coil to operate** the tag, **the power extractor having first and second terminals connected respectively to the first and second terminals of a winding of the transformer.

Neither Chatelot nor Ogita et al., separately or in combination, disclose the limitations shown in boldface.

Chatelot discloses data carrier 12 as having transmission-reception coil 14, transmission and reception circuits to be coupled to a resonant circuit to which coil 14 belongs, logic interposed

between the transmission and reception circuits, and a data memory or other digital supply. No structural details are provided. Chatelot, col. 2, lines 45-61. With no structural details for data carrier available 12 available, the examiner resorts to the structural details pertaining to Chatelot's reading-writing station 11 (the counterpart of appellants' reader) as the foundation for the rejection of claim 41 for a tag. 01/15/04 Office Action, p. 6.

Limitation [1]

Chatelot does not disclose the use of a transformer by either transmission circuit 11 or data carrier 12 in communicating with one another.

Ogita et al. discloses a transformer as a coupling device between a filter and an amplifier in a circuit for receiving radio waves. Ogita et al., Fig. 8. Ogita et al. does not envision the use of a single transformer in both transmitting and receiving signals and in power extraction as specified by Limitations [2], [3], [4], [5], and [6].

Thus, neither Chatelot nor Ogita et al. disclose a multi-purpose transformer as specified in claim 41.

Limitations [2] and [3]

Ogita et al. disclose capacitor 34 connected between first and second terminals of winding 32 of transformer 31 and antenna 21 connected between first and third terminals of the same winding. This is not in accordance with limitations [2] and [3] which requires the capacitor and coil to be connected to the same terminals. (The claim language specifies each winding has two terminals which are called "first terminal" and "second terminal". One may not assign the names

"first terminal" and "second terminal" to the terminals of winding 32 to which the coil of limitation [2] is connected and then change the assignment of names in interpreting limitation [3]. Instead, one should initially assign names such as "first terminal", "second terminal", and "third terminal" and use these names consistently in interpreting all of the limitations.)

Limitation [4]

Neither Chatelot nor Ogita et al. discloses a coil driver connected to a winding of a transformer. It would appear that there is no disclosure of limitation [4] by either of the references.

The examiner would presumably disagree. He would argue that Chatelot discloses a coil driver (transmission circuit 21) and Ogita et al. discloses a transformer (transformer 31) and it would be obvious to combine them in such a way as to satisfy limitation [4]. The examiner's proposed combination can be imagined by picturing a transformer inserted between capacitors 19 and coil 13 of Chatelot's Fig. 2. 01/15/04 Office Action, p. 5. But do we assume now that one of Chatelot's capacitors 19 corresponds to the capacitor of limitation [3]? If so, neither of capacitors 19 are connected across a winding of the transformer and limitation [3] is not satisfied. Moreover, the driver is not connected across a winding of the transformer and limitation [4] is not satisfied. The only solution is to get rid of Chatelot's capacitors 19 and replace them with a capacitor bridged across a winding of the transformer. And this would be a major revision of the Chatelot invention and unlikely to be an attractive option to one skilled in the art.

In short, neither Chatelot nor Ogita et al., separately or in combination, suggest limitation [4].

Limitation [5]

Ogita et al. discloses winding 33 connected to amplifier 37, the front end of a data extractor. The examiner would argue his combination of limitation [4] with Chatelot's reception circuit 22 substituted for transmission circuit 21 would satisfy limitation [5]. Again, the examiner's proposed combination can be imagined by picturing a transformer inserted between capacitors 19 and coil 13 of Chatelot's Fig. 2. 01/15/04 Office Action, p. 5.

However, the same questions arise here as discussed above in connection with limitation [4]. Do we assume now that one of Chatelot's capacitors 19 corresponds to the capacitor of limitation [3]? If so, neither of capacitors 19 are connected across a winding of the transformer and limitation [3] is not satisfied. Moreover, the data extractor is not connected across a winding of the transformer and limitation [5] is not satisfied. The only solution is to get rid of Chatelot's capacitors 19 and replace them with a capacitor bridged across a winding of the transformer. And again, this would be a major revision of the Chatelot invention and unlikely to be an attractive option to one skilled in the art.

In short, neither Chatelot nor Ogita et al., separately or in combination, suggest limitation [5].

Limitation [6]

And finally, neither Chatelot nor Ogita et al. disclose circuitry, either separately or in combination, which would correspond to the sixth limitation "a power extractor for extracting power from the signal induced in the coil to operate the tag, the power extractor having first and second terminals connected respectively to the first and second terminals of a winding of the transformer."

The examiner argues in response to appellants' arguments as follows:

"Regarding the 103 rejections of claim 41 (Chatelot and Kurusu or Ogita). The applicants argue that Chatelot does not show the limitations of element 1. This appears to be the only argument for this claim (with this rejection). One cannot show nonobviousness by attacking references individually where the rejections are abased on combinations of references." 01/15/04 Office Action, p. 20.

Neither Chatelot nor Ogita et al. nor the references in combination any of the six limitations specified in claim 41. Neither Chatelot nor Ogita et al. provide motivation to a person skilled in the art to attempt a combination of Chatelot and Ogita et al. that would result in applicants' claim-41 invention.

The examiner states that "it would have been obvious to one of ordinary skill in the art at the time of the invention to have used a transformer in the Chatelot system to provide isolation between the communication antenna coil and the other circuits in the reader as suggested by Ogita." 01/15/04 Office Action, p. 6.

Ogita et al does not suggest using a transformer to provide isolation. Ogita et al.'s transformer is simply a convenient way of matching impedances of loop antenna 21 and RF-amplifier 37. Ogita et al., col. 5, lines 41-48. Moreover, simply stating a possible reason for incorporating a transformer in Chatelot's invention is not sufficient to establish motivation:

> **"To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references."** *Ex parte Clapp*, 227 USPQ 972, 973 (Bd Pat. App. & Inter. 1985) (cited in MPEP § 2142).

The examiner has not established the *prima facie* obviousness of claim 41.

CLAIM 42

Claim 42 reads as follows:

42. The tag of claim 41 wherein the transformer has a first winding and a second winding, the capacitor, the coil driver, the data extractor, and the power extractor being connected to the first winding, the coil being connected to the second winding.

Chatelot discloses data carrier 12 as having transmission-reception coil 14, transmission and reception circuits to be coupled to a resonant circuit to which coil 14 belongs, logic interposed between the transmission and reception circuits, and a data memory or other digital supply. No structural details are provided. Chatelot, col. 2, lines 45-61. With no structural details for data carrier available 12 available, the examiner resorts to the structural details pertaining to Chatelot's reading-writing station 11 (the counterpart of appellants' reader) as the foundation for the rejection of claim 42 for a tag. 01/15/04 Office Action, p. 5.

Neither Chatelot nor Ogita et al. disclose "the capacitor, the coil driver, the data extractor, and the power extractor being connected to the first winding" nor do they disclose "the coil being connected to the second winding." The references also do not provide any motivation to a person skilled in the art to incorporate a transformer in Chatelot's invention for the purpose of achieving an invention with the limitations of claim 42.

The examiner did not address the specific limitations of claim 42 in either the 08/12/03 Office Action or the 01/15/04 Office Action. Nor did he refute the argument given above in the 01/15/04 Office Action. Instead, he commented as follows:

> "Regarding the 103 rejections of claim 42-45 (Chatelot and Kurusu or Ogita). Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references." 01/15/04 Office Action, p. 20.

Appellants' argument states very clearly that a transformer which interconnects a capacitor, a coil driver, a coil, a data extractor, and a power extractor as prescribed in the claim is not disclosed by either of the references. What more can be said without more meaningful responses from the examiner?

The examiner states that "it would have been obvious to one of ordinary skill in the art at the time of the invention to have used a transformer in the Chatelot system to provide isolation between the communication antenna coil and the other circuits in the reader as suggested by Ogita." 01/15/04 Office Action, p. 6.

Ogita et al does not suggest using a transformer to provide isolation. Ogita et al.'s transformer is simply a convenient way of matching impedances of loop antenna 21 and RF-amplifier 37. Ogita et al., col. 5, lines 41-48. Moreover, simply stating a possible reason for incorporating a transformer in Chatelot's invention is not sufficient to establish motivation:

> **"To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention**

or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." *Ex parte Clapp*, 227 USPQ 972, 973 (Bd Pat. App. & Inter. 1985) (cited in MPEP § 2142).

The examiner has not established the *prima facie* obviousness of claim 42.

CLAIM 44

Claim 44 reads as follows:

44. The tag of claim 41 wherein the transformer has a first winding, a second winding, and a third winding, the capacitor and the coil driver being connected to the first winding, the data extractor and the power extractor being connected to the second winding, and the coil being connected to the third winding.

Chatelot discloses data carrier 12 as having transmission-reception coil 14, transmission and reception circuits to be coupled to a resonant circuit to which coil 14 belongs, logic interposed between the transmission and reception circuits, and a data memory or other digital supply. No structural details are provided. Chatelot, col. 2, lines 45-61. With no structural details for data carrier available 12 available, the examiner resorts to the structural details pertaining to Chatelot's reading-writing station 11 (the counterpart of appellants' reader) as the foundation for the rejection of claim 44 for a tag. 01/15/04 Office Action, p. 5.

Neither Chatelot nor Ogita et al. disclose "the capacitor and the coil driver being connected to the first winding, the data extractor, and the power extractor being connected to the second winding, and the coil being connected to the third winding." The references also do not provide any

motivation to a person skilled in the art to incorporate a transformer in Chatelot's invention for the purpose of achieving an invention with the limitations of claim 44.

The examiner did not address the specific limitations of claim 44 in either the 08/12/03 Office Action or the 01/15/04 Office Action. Nor did he refute the argument given above in the 01/15/04 Office Action. Instead, he commented as follows:

> "Regarding the 103 rejections of claim 42-45 (Chatelot and Kurusu or Ogita). Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references." 01/15/04 Office Action, p. 20.

Appellants' argument states very clearly that a transformer which interconnects a capacitor, a coil driver, a coil, a data extractor, and a power extractor as prescribed in the claim is not disclosed by either of the references. What more can be said without more meaningful responses from the examiner?

The examiner states that "it would have been obvious to one of ordinary skill in the art at the time of the invention to have used a transformer in the Chatelot system to provide isolation between the communication antenna coil and the other circuits in the reader as suggested by Ogita." 01/15/04 Office Action, p. 6.

Ogita et al does not suggest using a transformer to provide isolation. Ogita et al.'s transformer is simply a convenient way of matching impedances of loop antenna 21 and RF-amplifier 37. Ogita et al., col. 5, lines 41-48. Moreover, simply stating a possible reason for incorporating a transformer in Chatelot's invention is not sufficient to establish motivation:

"To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." *Ex parte Clapp*, 227 USPQ 972, 973 (Bd Pat. App. & Inter. 1985) (cited in MPEP § 2142).

The examiner has not established the *prima facie* obviousness of claim 44.

CLAIM 45

Claim 45 reads as follows:

45. The tag of claim 41 wherein the transformer has a first winding, a second winding, a third winding, and a fourth winding, the capacitor and the coil driver being connected to the first winding, the data extractor being connected to the second winding, the power extractor being connected to the third winding, and the coil being connected to the fourth winding.

Chatelot discloses data carrier 12 as having transmission-reception coil 14, transmission and reception circuits to be coupled to a resonant circuit to which coil 14 belongs, logic interposed between the transmission and reception circuits, and a data memory or other digital supply. No structural details are provided. Chatelot, col. 2, lines 45-61. With no structural details for data carrier available 12 available, the examiner resorts to the structural details pertaining to Chatelot's reading-writing station 11 (the counterpart of appellants' reader) as the foundation for the rejection of claim 45 for a tag. 01/15/04 Office Action, p. 5.

Neither Chatelot nor Ogita et al. disclose "the capacitor and the coil driver being connected to the first winding, the data extractor being connected to the second winding, the power extractor

being connected to the third winding, and the coil being connected to the fourth winding." The references also do not provide any motivation to a person skilled in the art to incorporate a transformer in Chatelot's invention for the purpose of achieving an invention with the limitations of claim 45.

The examiner did not address the specific limitations of claim 45 in either the 08/12/03 Office Action or the 01/15/04 Office Action. Nor did he refute the argument given above in the 01/15/04 Office Action. Instead, he commented as follows:

> "Regarding the 103 rejections of claim 42-45 (Chatelot and Kurusu or Ogita). Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references." 01/15/04 Office Action, p. 20.

Appellants' argument states very clearly that a transformer which interconnects a capacitor, a coil driver, a coil, a data extractor, and a power extractor as prescribed in the claim is not disclosed by either of the references. What more can be said without more meaningful responses from the examiner?

The examiner states that "it would have been obvious to one of ordinary skill in the art at the time of the invention to have used a transformer in the Chatelot system to provide isolation between the communication antenna coil and the other circuits in the reader as suggested by Ogita." 01/15/04 Office Action, p. 6.

Ogita et al does not suggest using a transformer to provide isolation. Ogita et al.'s transformer is simply a convenient way of matching impedances of loop antenna 21 and RF-

amplifier 37. Ogita et al., col. 5, lines 41-48. Moreover, simply stating a possible reason for incorporating a transformer in Chatelot's invention is not sufficient to establish motivation:

> **"To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references."** *Ex parte Clapp*, 227 USPQ 972, 973 (Bd Pat. App. & Inter. 1985) (cited in MPEP § 2142).

The examiner has not established the *prima facie* obviousness of claim 45.

VII. WHETHER CLAIMS 5-13, 25, 47-60, AND 62-64 ARE UNPATENTABLE UNDER 35 U.S.C. § 103(A) IN VIEW OF CARROLL ET AL. (U.S. 5,517,194).

CLAIM 5

Claim 5 reads as follows:

5. A reader for use with a tag, the reader comprising:

a coil;

[1] at least one capacitor;

[2] a means for coupling the capacitor(s) to the coil;

[3] a means for driving the coil through the capacitor(s) with a driving signal;

a means for generating the driving signal;

[4] a means for embedding a bit-timing clock signal in the driving signal;

a means for embedding a sequence of bits to be communicated to a tag in the driving signal.

Carroll et al. does not disclose any of the limitations shown in boldface above.

Limitations [1], [2], and [3]

Carroll et al. utilizes microprocessor 12 to directly drive coil 18 by means of coil drive circuit 16. No capacitor is involved in the process. Carroll et al., col. 6, lines 7-9. Thus, Carroll et al. does not disclose limitations [1], [2], and [3].

The examiner argues that it would be obvious to a person skilled in the art to incorporate Carroll et al.'s tuning capacitor 44 in transponder 40 (Carroll et al., Fig. 3) as a feed-through capacitor from coil drive 16 to coil 18 in controller 10 (Carroll et al., Fig. 1) in order to provide

tuning. But if a person skilled in the art wanted to follow Carroll et al.'s example, he would connect a tuning capacitor across coil 18 in controller 10—just like the tuning capacitor in transponder 40 is connected. And connecting a capacitor ACROSS the coil does not enable a "means" to drive a coil with a driving signal through a capacitor connected to the coil (Limitations [1], [2], and [3]).

The use of a tuning capacitor connected across the coil in transponder 40 is not a disclosure of the use of a coupling capacitor between a driving means (coil drive 16) and a coil (coil 18) in controller 10. Nor would the presence of a coil and capacitor connected in parallel in transponder 40 suggest to a person skilled in the art that a coupling capacitor should be used in connecting the drive means to the coil in controller 10.

Limitation [4]

Please see the discussion under the **ISSUE IV, CLAIM 70** heading for an argument in support of the assertion that Carroll et al. does not disclose Limitation [4], "a means for embedding a bit-timing clock signal in the driving signal" including an argument based on an *In re Donaldson Co.* construal of the claim language.

Carroll et al. <u>does</u> disclose transponder 40 (the counterpart of appellants' "tag") embedding a bit-timing clock signal in the signal returned by transponder 40 to controller 10. However, there is no basis for arguing that a person skilled in the art would find it obvious to also embed a bit-timing clock signal in the driving signal transmitted by controller 10 to transponder 40. A person skilled in the art would recognize that it was unnecessary for both controller 10 and transponder 40 to embed bit-timing clock signals in their transmissions. Carroll et al., being aware of the technological

realities, did NOT have controller 10 embed a bit-timing clock signal in the controller 10 transmission.

Carroll et al. does not "teach or suggest all the claim limitations" of claim 5 and prima facie obviousness of claim 5 has not been established.

CLAIM 6

Claim 6 reads as follows:

6. *The reader of claim 5 wherein the means for embedding a sequence of bits comprises: a means for causing the phase of the driving signal to have a first phase when a "0" bit is being transmitted and to have a second phase when a "1" bit is being transmitted.*

Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal. Controller 10 embeds a sequence of bits in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not a teaching of the claim-6 limitation.

The examiner seems to argue that because Carroll et al.'s transponder 40 responds to controller 10's interrogation with a PSK signal, a person skilled in the art would be motivated to change controller 10's means for communicating data to transponder 40 to PSK. However, there is no suggestion in Carroll et al. or in the knowledge generally available to one of ordinary skill in the art to make such a change. Carroll et al. chose the simple means of varying the frequency of the driving signal for communicating data from controller 10 to transponder 40 because the detection

of frequency changes is particularly simple and does not require a bit-timing clock signal to be available in transponder 40 thereby resulting in a less-complicated and less-costly transponder.

There is no motivation for changing controller 10's method of transmitting data to transponder 40, and consequently, prima facie obviousness of applicants' claim-6 invention has not been established.

The above argument was first presented to the examiner in appellants' response to the 04/04/03 Office Action. In response to appellants' arguments that motivation is lacking for changing Carroll et al.'s preferred FSK mode of communication from controller 10 to transponder 40 to PSK, the examiner made the following statement:

> "While Carroll does in fact teach using FSK to communicate data to the tag, Carroll also teaches the use of PSK to transmit data. It is well within the skill in the art to choose between transmission encoding schemes to provide optimal transmission methods. Does the applicant actually believe that they invented the use of PSK in a communication?" 08/12/03 Office Action, p. 22.

Appellants' responded to the 08/12/03 Office Action by repeating the argument given above and adding the following.

The fact that "it is well within the skill in the art to choose transmission encoding schemes" does not qualify as motivation:

> **"At best, the examiner's comments regarding obviousness amount to an assertion that one of ordinary skill in the relevant art would have been able to arrive at appellant's invention because he had the necessary skills to carry out the requisite process steps. This is an inappropriate standard for obviousness. See *Orthokinetics Inc. v. Safety Travel Chairs Inc.*, 806 F.2d 1565, 1 USPQ2d 1081 (Fed. Cir. 1986). That which is within the capabilities of one skilled in the art is not synonymous with obviousness. *Ex parte Gerlach*, 212 USPQ 471 (Bd.App. 1980). See also footnote 16 of *Panduit Corp.***

v. Dennison Mfg. Co., 774 F.2d 1082, 1092, 227 USPQ 337, 343 (Fed. Cir. 1985)." *Ex parte Levengood*, 28 USPQ2d 1300, 1301 (Bd. Pat. App. & Inter. 1993).

The examiner in his 01/15/04 Office Action repeated his 08/12/03 response (as above except for omitting the question "Does the applicant actually believe that they invented the use of PSK in a communication?") and added the following.

> "The applicant states that because something is well known, that is not sufficient motivation. The examiner did not rely on the fact that PSK is well known for motivation, the rejection above and repeated here states that changing between known schemes would optimize transmissions." 01/15/04 Office Action, pp 21-22.

The examiner seems to be saying that a person skilled in the art would be motivated to completely revamp the Carroll et al. invention by changing the technique used to transmit information from controller 10 to transponder 40 from FSK to PSK because "changing between known schemes would optimize transmissions." This is hardly the convincing argument called for by *In re Clapp*:

> **"To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references."** *Ex parte Clapp*, 227 USPQ 972, 973 (Bd Pat. App. & Inter. 1985) (cited in MPEP § 2142).

The examiner has not established the *prima facie* obviousness of claim 6.

CLAIM 7

Claim 7 reads as follows:

7. *The reader of claim 5 wherein the means for embedding a sequence of bits comprises:*

a means for modulating the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 7.

Carroll et al.'s controller 10 transmits data by changing the frequency of the driving signal. Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al., col. 3, lines 45-62. This is not the same as generating "a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted" and then using this "periodic signal" to modulate the driving signal.

Carroll et al. does not teach the limitation of claim 7, and there is no motivation for changing controller 10's method of transmitting data to transponder 40.

The above argument was first presented to the examiner in appellants' response to the 04/04/03 Office Action. In response to appellants' arguments that motivation is lacking for changing Carroll et al.'s mode of communication from controller 10 to transponder 40, the examiner argued that "[i]t is well within the skill in the art to choose between transmission encoding schemes to provide optimal transmission methods." 08/12/03 Office Action, p. 22.

Appellants responded to the 08/12/03 Office Action by repeating the argument given above and adding the following.

The fact that "it is well within the skill in the art to choose transmission encoding schemes" does not qualify as motivation. *Ex parte Levengood*, 28 USPQ2d 1300, 1301 (Bd. Pat. App. & Inter. 1993.

The examiner in his 01/15/04 Office Action again said that "[i]t is well within the skill in the art to choose between transmission encoding schemes to provide optimal transmission methods." He attempted to rebut appellants' arguments as follows:

> "The applicant argues that Carroll's PSK is a reversal of the phase of the driving signal and therefore not a periodic signal having a first phase when a "0" is transmitted and a second phase when a "1" is transmitted. While there may be times in Carroll's transmission when these "0" and "1" rules do not apply there are times when these rules do apply. All that is required by the claim is that a "0" be identified (at least once) by a first phase and a "1" be identified (at least once) by a second phase, this is shown by Carroll. The signal of Carroll is periodic in that it has a steady bit period." 01/15/04 Office Action, pp 21-22.

The problem with the examiner's rebuttal is that it is an attempt to refute an argument that appellants never made. Appellants' argument, which has consistently been made in responding to the 04/04/03 Office Action, the 08/12/03 Office Action, and the 01/15/04 Office Action (by means of this Appeal Brief) is as follows:

> "Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al., col. 3, lines 45-62. This is not the same as generating "a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted" and then using this "periodic signal" to modulate the driving signal."

The examiner converts this paragraph to the following:

"The applicant argues that Carroll's PSK is a reversal of the phase of the driving signal and therefore not a periodic signal having a first phase when a "0" is transmitted and a second phase when a "1" is transmitted."

Note how the examiner has ignored the words "and then using this 'periodic signal' to modulate the driving signal."

Appellants' reiterate, Carroll et al. does not disclose, either in connection with controller 10 or transponder 40, the modulation technique specified in claim 7

Carroll et al. does not disclose the claim-7 invention and even if it were disclosed, there is no motivation to be found in Carroll et al. or general knowledge for incorporating the technique in the Carroll et al. invention.

Prima facie obviousness of claim 7 has not been established.

CLAIM 8

Claim 8 reads as follows:

8. The reader of claim 5 wherein the means for embedding a sequence of bits comprises: a means for modulating the amplitude of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 8.

Carroll et al.'s controller 10 transmits data by changing the frequency of the driving signal. Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al., col. 3, lines 45-62. This is not the same as generating "a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted" and then using this "periodic signal" to amplitude modulate the driving signal.

Carroll et al. does not teach the limitation of claim 8, and there is no motivation for changing controller 10's method of transmitting data to transponder 40.

In response to applicants' arguments that motivation is lacking for changing Carroll et al.'s mode of communication from controller 10 to transponder 40, the examiner argues that "[i]t is well within the skill in the art to choose between transmission encoding schemes to provide optimal transmission methods." 01/15/04 Office Action, p. 21.

The fact that "it is well within the skill in the art to choose transmission encoding schemes" does not qualify as motivation. *Ex parte Levengood*, 28 USPQ2d 1300, 1301 (Bd. Pat. App. & Inter. 1993.

Prima facie obviousness of claim 8 has not been established.

CLAIM 9

Claim 9 reads as follows:

9. The reader of claim 5 wherein the means for embedding a sequence of bits comprises: a means for modulating the phase of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 9.

Carroll et al.'s controller 10 transmits data by changing the frequency of the driving signal. Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al., col. 3, lines 45-62. This is not the same as generating "a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted" and then using this "periodic signal" to phase modulate the driving signal.

Carroll et al. does not teach the limitation of claim 9, and there is no motivation for changing controller 10's method of transmitting data to transponder 40.

In response to applicants' arguments that motivation is lacking for changing Carroll et al.'s mode of communication from controller 10 to transponder 40, the examiner argues that "[i]t is well within the skill in the art to choose between transmission encoding schemes to provide optimal transmission methods." 01/15/04 Office Action, p. 21.

The fact that "it is well within the skill in the art to choose transmission encoding schemes" does not qualify as motivation. *Ex parte Levengood*, 28 USPQ2d 1300, 1301 (Bd. Pat. App. & Inter. 1993.

Prima facie obviousness of claim 9 has not been established.

CLAIM 10

Claim 10 reads as follows:

10. The reader of claim 5 wherein the means for embedding a sequence of bits comprises: a means for causing the phase of the driving signal to have a first frequency when a "0" bit is being transmitted and to have a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 10.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as "causing the phase of the driving signal to have a first frequency when a "0" bit is being transmitted and to have a second frequency when a "1" bit is being transmitted" .

Carroll et al. does not teach the limitation of claim 10, and there is no motivation for changing controller 10's method of transmitting data to transponder 40.

In response to applicants' arguments that motivation is lacking for changing Carroll et al.'s mode of communication from controller 10 to transponder 40, the examiner argues that "[i]t is well within the skill in the art to choose between transmission encoding schemes to provide optimal transmission methods." 01/15/04 Office Action, p. 21.

The fact that "it is well within the skill in the art to choose transmission encoding schemes" does not qualify as motivation. *Ex parte Levengood*, 28 USPQ2d 1300, 1301 (Bd. Pat. App. & Inter. 1993.

Prima facie obviousness of claim 10 has not been established.

CLAIM 11

Claim 11 reads as follows:

11. The reader of claim 5 wherein the means for embedding a sequence of bits comprises: a means for modulating the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 11.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as generating "a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted" and then modulating the driving signal with this periodic signal.

Carroll et al. does not teach the limitation of claim 11, and there is no motivation for changing controller 10's method of transmitting data to transponder 40.

In response to applicants' arguments that motivation is lacking for changing Carroll et al.'s mode of communication from controller 10 to transponder 40, the examiner argues that "[i]t is well within the skill in the art to choose between transmission encoding schemes to provide optimal transmission methods." 01/15/04 Office Action, p. 21.

The fact that "it is well within the skill in the art to choose transmission encoding schemes" does not qualify as motivation. *Ex parte Levengood*, 28 USPQ2d 1300, 1301 (Bd. Pat. App. & Inter. 1993.

Prima facie obviousness of claim 11 has not been established.

CLAIM 12

Claim 12 reads as follows:

12. The reader of claim 5 wherein the means for embedding a sequence of bits comprises: a means for modulating the amplitude of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 12.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to

send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as generating "a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted" and then amplitude-modulating the driving signal with this periodic signal.

The above argument was first presented to the examiner in appellants' response to the 04/04/03 Office Action. The examiner responded to the argument with the statement: "What the applicant claims is FSK. Carroll discloses FSK for the claimed link between the reader and the tag." 08/12/03 Office Action, pp. 22-23.

Appellants responded to the 08/12/03 Office Action with the following.

The examiner ignores the differences in the frequency modulation claimed by applicants and the frequency modulation disclosed by Carroll et al. The examiner is incorrect in substituting his interpretation of the claim language for the actual claim language. All of the words in the claim must be considered:

> **"To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). All words in a claim must be considered in judging the patentability of that claim against the prior art. *In re Wilson*, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970)." MPEP § 2143.03.**

Carroll et al. does not teach the limitation of claim 12, and there is no motivation for changing controller 10's method of transmitting data to transponder 40.

The examiner responded to the above with the following remarks.

"The applicant argues that Carroll does not transmit a periodic signal having a first frequency to represent a "0" and a second frequency to represent a "1". What the applicant claims is FSK. The

applicant argues that examiner is incorrect in this interpretation, yet offers no explanation of why." 01/15/04 Office Action, p. 22.

As in the case of claim 7, the examiner does not consider all of the claim language in his analysis. Appellants' argument, which has consistently been made in responding to the 04/04/03 Office Action, the 08/12/03 Office Action, and the 01/15/04 Office Action (by means of this Appeal Brief) is as follows:

> "Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as generating "a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted" and then amplitude-modulating the driving signal with this periodic signal."

The examiner interprets appellants argument in the following way:

> "The applicant argues that Carroll does not transmit a periodic signal having a first frequency to represent a "0" and a second frequency to represent a "1". What the applicant claims is FSK. The applicant argues that examiner is incorrect in this interpretation, yet offers no explanation of why."

What the examiner has failed to see is that there are two "signals" referred to in the claim language—a "driving signal" and a "periodic signal". The claim states that a "periodic signal" is frequency shift keyed (FSK) with the bits to be transmitted and the resulting frequency shift keyed "periodic signal" modulates the amplitude of the "driving signal". Carroll et al. frequency shift keys a "driving signal".

with the bits to be transmitted with no involvement of a "periodic signal". Thus, Carroll et al. does not disclose appellants' claim-12 invention.

Prima facie obviousness of claim 12 has not been established.

CLAIM 13

Claim 13 reads as follows:

13. The reader of claim 5 wherein the means for embedding a sequence of bits comprises: a means for modulating the phase of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 13.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as generating "a periodic signal having a first freqűency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted" and then phase modulating the driving signal with this periodic signal.

The above argument was first presented to the examiner in appellants' response to the 04/04/03 Office Action. The examiner responded to the argument with the statement: "What the applicant claims is FSK. Carroll discloses FSK for the claimed link between the reader and the tag." 08/12/03 Office Action, pp. 22-23.

Appellants responded to the 08/12/03 Office Action with the following.

The examiner ignores the differences in the frequency modulation claimed by applicants and the frequency modulation disclosed by Carroll et al. The examiner is incorrect in substituting his interpretation of the claim language for the actual claim language. All of the words in the claim must be considered:

> **"To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). All words in a claim must be considered in judging the patentability of that claim against the prior art. *In re Wilson*, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970)." MPEP § 2143.03.**

Carroll et al. does not teach the limitation of claim 13, and there is no motivation for changing controller 10's method of transmitting data to transponder 40.

The examiner responded to the above with the following remarks.

"The applicant argues that Carroll does not transmit a periodic signal having a first frequency to represent a "0" and a second frequency to represent a "1". What the applicant claims is FSK. The applicant argues that examiner is incorrect in this interpretation, yet offers no explanation of why." 01/15/04 Office Action, p. 22.

As in the case of claim 7, the examiner does not consider all of the claim language in his analysis. Appellants' argument, which has consistently been made in responding to the 04/04/03

Office Action, the 08/12/03 Office Action, and the 01/15/04 Office Action (by means of this Appeal Brief) is as follows:

> "Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as generating "a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted" and then phase-modulating the driving signal with this periodic signal."

The examiner interprets appellants argument in the following way:

> "The applicant argues that Carroll does not transmit a periodic signal having a first frequency to represent a "0" and a second frequency to represent a "1". What the applicant claims is FSK. The applicant argues that examiner is incorrect in this interpretation, yet offers no explanation of why."

What the examiner has failed to see is that there are two "signals" referred to in the claim language—a "driving signal" and a "periodic signal". The claim states that a "periodic signal" is frequency shift keyed (FSK) with the bits to be transmitted and the resulting frequency shift keyed "periodic signal" modulates the phase of the "driving signal". Carroll et al. frequency shift keys a "driving signal" with the bits to be transmitted with no involvement of a "periodic signal". Thus, Carroll et al. does not disclose appellants' claim-13 invention.

Prima facie obviousness of claim 13 has not been established.

CLAIM 25

Claim 25 reads as follows:

*25. A reader for use with **[1] a tag that transmits a periodic signal having a first frequency when a "0" bit is to be communicated and a second frequency when a "1" bit is to be communicated**, the reader comprising:*

a means for receiving the tag signal;

[2] a means for measuring the period of each cycle of the signal received from the tag during a bit period.

Carroll et al. does not teach either of the limitations shown in boldface.

Limitation [1]

Carroll et al. discloses controller 10 which can be used with transponder 40 which utilizes a phase-coherent Manchester encoded PSK RF signal to send data. Carroll et al., col. 15, lines 54-56. Carroll et al. does not teach a reader that can be used with "a tag that transmits a periodic signal having a first frequency when a "0" bit is to be communicated and a second frequency when a "1" bit is to be communicated."

The examiner made the following argument in the 08/12/03 Office Action: "What the applicant claims is FSK. Carroll discloses FSK for the claimed link between the reader and the tag." 08/12/03 Office Action, pp. 22-23.

Appellants responded to the examiner's argument as follows.

The examiner ignores the differences in the frequency modulation claimed by applicants and the frequency modulation disclosed by Carroll et al. The examiner is incorrect in substituting his interpretation of the claim language for the actual claim language. All of the words in the claim must be considered:

> **"To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). All words in a claim must be considered in judging the patentability of that claim against the prior art. *In re Wilson*, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970)." MPEP § 2143.03.**

The examiner responded to this argument as follows:

> "Regarding the 103 rejections of claims 12, 13, 25 (Carroll). The applicant argues that Carroll does not transmit a periodic signal having a first frequency to represent a "0" and a second frequency to represent a "1". What the applicant claims is FSK. the applicant argues that examiner is incorrect in this interpretation, yet offers no explanation of why. It remains the position of the examiner that the claims. [*sic*] Carroll discloses FSK for the claimed link between the reader and the tag. The applicant's claims are not as narrow as their arguments. The claims us [*sic*] open language, and since **Carroll uses a periodic signal having a first frequency to represent a "0" and a second frequency to represent a "1"** Carroll reads on the claim." 01/15/04 Office Action, p. 22.

The examiner's error in comparing Carroll et al.'s disclosure with the claim language arises as a result of his misreading of Carroll et al. (shown in boldface in the last sentence above). It was pointed out to the examiner in appellants' response to the 08/12/03 Office Action under the **CLAIM 11, CLAIM 12,** and **CLAIM 13** headings that:

"Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit." Carroll et al., col. 7, lines 25-29.

"Changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit" is not the same as transmitting "a second frequency when a "1" bit is to be communicated."

Carroll et al. does not disclose the particular FSK modulation technique specified in claim 25 for transmitting data in either direction between controller 10 to transponder 40.

Even if the FSK modulation technique of claim 25 had been disclosed for the transmission of data from controller 10 to transponder 40, why would a person skilled in the art be motivated to change the Manchester encoded PSK link from transponder 40 to controller 10 to FSK? Such a change would require a complete redesign of both controller 10 and transponder 40 and for what purpose?

The examiner argues that a preamble limitation is "generally not accorded any patentable weight where it merely recites the purpose of a process or the intended used of a structure and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone." 08/12/03 Office Action, p. 13.

Limitation [1] does not merely recite an intended use of the reader. The primary function of a reader is to "read" the data transmitted by a tag. To do this, the structure of the reader must be

tailored to the method used by the tag to transmit data. Thus, limitation [1] is clearly a limitation on the structure of the reader that cannot be ignored.

Limitation [2]

Carroll et al.'s controller 10 anticipates receiving a phase-modulated 62.5-kHz signal from transponder 40 (Carroll et al., Fig. 3). Carroll et al. does not need to measure the period of the received signal nor does it disclose performing such an operation

Carroll et al. does not teach the limitations of claim 25, and there is no motivation for changing controller 10's method of receiving data from transponder 40.

Prima facie obviousness of claim 25 has not been established.

CLAIM 47

Claim 47 reads as follows:

47. A tag for use with a reader, the reader communicating a sequence of bits to the tag by transmitting a first signal during a bit period when a "0" bit is to be communicated and a second signal during a bit period when a "1" is to be communicated, [1] the reader embedding a bit-timing clock signal in the transmitted signals, the tag comprising:

a coil;

a capacitor;

a means for coupling the capacitor to the coil and coupling the coil to at least one other means, the signal(s) provided to the other means as a result of the coupling being called coupling-

means signal(s), the combination of the coil, the capacitor, and the coupling means being called the resonating circuit;

[2] a means for generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded in the transmitted signals;

[3] a means for identifying the bit being transmitted during each bit period, the beginning and ending of each bit period being indicated by the bit-timing clock signal.

Carroll et al. does not disclose any of the limitations in boldface.

Limitation [1]

Limitation [1] is not disclosed by Carroll et al. For details, please see discussion under the ISSUE IV, CLAIM 70 heading.

The examiner argues that a preamble limitation is "generally not accorded any patentable weight where it merely recites the purpose of a process or the intended used of a structure and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone." 08/12/03 Office Action, p. 13.

Limitation [1] does not merely recite an intended use of the tag. One of the primary functions of a tag is to "read" the data transmitted by a reader. To do this, the structure of the tag must be tailored to the method used by the reader to transmit data. Thus, limitation [1] is clearly a limitation on the structure of the tag that cannot be ignored.

Limitation [2]

Carroll et al.'s controller 10 does not transmit a bit-timing clock signal to transponder 40 (see discussion under **ISSUE IV, CLAIM 70** heading). Consequently, there is no bit-timing clock signal originating in controller 10 that could be used by transponder 40 to synchronize its own bit-timing clock. For additional discussion of this limitation, see **ISSUE IV, CLAIM 74,** ***Limitation [2].***

Carroll et al. does not teach Limitation [2].

Limitation [3]

Carroll et al.'s transponder 40 has no information available from controller 10 as to the beginning and ending of a bit period and therefore does not teach the use of this information in identifying the bit being transmitted during the bit period.

The examiner argues that "[t]he sync generator 70 is synchronized to the received clock signal since the timing control element 60 drives all the elements that follow, etc 64,48,68 and 70." 08/12/03 Office Action, p. 18. The "received clock signal" that the examiner refers to is presumably the FSK modulated signal of frequency 125 kHz from controller 10. col. 7, lines 22-25; col. 17, lines 39-52. This is the carrier of the data that controller 10 transmits to transponder 40. It is not a bit-timing clock signal to which the bit-timing clock signal generated by transponder 40 is synchronized.

Carroll et al. does not teach Limitation [3].

Carroll et al. does not teach the boldface limitations of claim 47, and there is no motivation for incorporating the limitations in Carroll et al.'s controller 10 and transponder 40.

Prima facie obviousness of claim 47 has not been established.

CLAIM 48

Claim 48 reads as follows:

48. The tag of claim of 47 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the coupling-means signal;

a means for translating the weighted integration(s) into a bit value.

Carroll et al. does not even mention the term "weighted integration" let alone teaching its use in determining bit values in accordance with the claim-48 limitation.

Carroll et al. does not teach the limitation of claim 48, and there is no motivation for incorporating the limitation in Carroll et al.'s transponder 40.

Prima facie obviousness of claim 48 has not been established.

The examiner responded to applicants' assertion that there is no disclosure of the limitation in Carroll et al. and that there is no motivation for a person skilled in the art to incorporate such a limitation in Carroll et al.'s invention by stating:

> "Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references." 08/12/03 Office Action, p. 23-24.

Appellants responded to the examiner's argument in their response to 08/12/03 Office Action as follows:

> "Applicants' argument is not a general allegation. The argument is very specific in stating that the claim limitation is not disclosed in the reference. And in two office actions, the

examiner has failed to rebut applicants' argument. Moreover, the examiner has not established motivation on the part of a person skilled in the art to modify the referenced invention to include the limitation.

"The examiner is reminded that in rejecting a claim for obviousness, he 'should set forth in the Office action (A) The relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate, (B) The difference or differences in the claim over the applied references(s), (C) The proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter, and (D) an explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification.' MPEP § 706.02(j)."

CLAIM 49

Claim 49 reads as follows:

49. The tag of claim of 47 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the amplitude of the coupling-means signal;

a means for translating the weighted integration(s) into a bit value.

The examiner argues that "amplitude shift keying is a common alternative to phase shift keying or frequency shift keying, and to have substituted this type of modulation scheme for that used in Carroll would not have involved an unobvious step." 08/12/03 Office Action, p. 9. There

is no mention of amplitude shift keying in claim 49 or in claim 47 from which claim 49 depends. It would appear that the examiner's comment is irrelevant insofar as the patentability of applicants' claim-49 invention is concerned.

Carroll et al. does not even mention the term "weighted integration" let alone teaching its use in determining bit values in accordance with the claim-49 limitations. The examiner argues that [d]ividing by 64 is weighted integration for providing the claimed feature. 08/12/03 Office Action, p. 24. The divide-by-64 timing control 60 is simply a synchronous counter (col. 18, lines 58-60). It has nothing to do with performing a weighted integration of a received signal. A weighted integration results from the multiplication of the signal received during a bit period by a weighting function and integrating the result.

Carroll et al. does not teach the limitations of claim 49, and there is no motivation for incorporating these limitations in Carroll et al.'s transponder 40.

Prima facie obviousness of claim 49 has not been established.

CLAIM 50

Claim 50 reads as follows:

50. The tag of claim of 47 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the phase of the coupling-means signal;

a means for translating the weighted integration(s) into a bit value.

Carroll et al. does not even mention the term "weighted integration" let alone teaching its use in determining bit values in accordance with the claim-50 limitations. The examiner argues that [d]ividing by 64 is weighted integration for providing the claimed feature.. 08/12/03 Office Action, p. 24. The divide-by-64 timing control 60 is simply a synchronous counter (col. 18, lines 58-60). It has nothing to do with performing a weighted integration of a received signal. A weighted integration results from the multiplication of the signal received during a bit period by a weighting function and integrating the result.

Carroll et al. does not teach the limitations of claim 50, and there is no motivation for incorporating these limitations in Carroll et al.'s transponder 40.

Prima facie obviousness of claim 50 has not been established.

CLAIMS 51-55

Claims 51-55 reads as follows:

51. The tag of claim 47 wherein the first signal is a periodic signal with a first value for a predetermined signal parameter and the second signal is the periodic signal with a second value for the predetermined signal parameter, the predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the periodic signal, the bit-identifying means comprising:

a means for generating a first replica of the periodic signal with the first value for the predetermined signal parameter and a second replica of the periodic signal with the second value for the predetermined signal parameter;

a means for multiplying the coupling-means signal by the first replica thereby obtaining a first product waveform and by the second replica thereby obtaining a second product waveform;

a means for integrating the first and second product waveforms for a bit period and translating the integration results into a bit value.

52. *The tag of claim 47 wherein the first signal is a periodic signal with a first value for a first predetermined signal parameter and the second signal is the periodic signal with a second value for the first predetermined signal parameter, the first predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the periodic signal, the periodic signal modulating a second predetermined signal parameter of a carrier signal, the second predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the carrier signal, the bit-identifying means comprising:*

a means for demodulating the second predetermined signal parameter of the coupling-means signal;

a means for generating a first replica of the periodic signal with the first value for the first predetermined signal parameter and a second replica of the periodic signal with the second value for the first predetermined signal parameter;

a means for multiplying the demodulated coupling-means signal by the first replica thereby obtaining a first product waveform and by the second replica thereby obtaining a second product waveform;

a means for integrating the first and second product waveforms for a bit period and translating the integration results into a bit value.

53. The tag of claim 47 wherein the bit-identifying means comprises:

a means for generating replicas of the first and second signals transmitted by the reader;

a means for obtaining the amplitude of a coupling-means signal as a function of time;

a means for multiplying the coupling-means signal amplitude by the replica of the first signal to obtain a first product signal and by the replica of the second signal to obtain a second product signal;

a means for integrating the first product signal over a bit period to obtain a first integration and integrating the second product signal over a bit period to obtain a second integration;

a means for translating the first and second integrations into a bit value.

54. The tag of claim 47 wherein the means for generating a bit-timing clock signal that indicates the start of each bit period comprises:

a means for generating a clock signal having a bit-start indicator during each bit period, the bit-start indicators being adjustable in time;

a means for recognizing the bit transition in the coupling-means signal from one bit to the next;

a means for adjusting the bit-start indicators until the bit-start indicators and the bit transitions in the coupling-means signal occur simultaneously.

55. The tag of claim 47 wherein the reader embeds a bit-timing clock signal in the transmitted signals by initially alternating the transmission of the first signal and the second

signal, the means for generating a bit-timing clock signal that indicates the start of each bit period comprising:

a means for generating a clock signal having a bit-start indicator during each bit period, the bit-start indicators being adjustable in time;

a means for recognizing the bit transitions in the coupling-means signal resulting from the transitions from the first signal to the second signal and from the second signal to the first signal;

a means for adjusting the bit-start indicators until the bit-start indicators and the transitions in the coupling-means signal occur simultaneously.

Carroll et al. does not teach the limitations shown in boldface, and there is no motivation for incorporating these limitations in Carroll et al.'s transponder 40.

Prima facie obviousness of claims 51-55 have not been established.

The examiner responded to appellants' assertion that there is no disclosure of these limitations in Carroll et al. and that there is no motivation for a person skilled in the art to incorporate these limitations in Carroll et al.'s invention by stating:

> "Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references."
>
> 08/12/03 Office Action, p. 23-24.

Appellants responded to the above as follows.

Applicants' argument is not a general allegation. The argument is very specific in stating that the claim limitations shown in boldface are not disclosed in the reference. And in two office actions, the examiner has failed to rebut applicants' argument. Moreover, the examiner has not established motivation on the part of a person skilled in the art to modify the referenced invention to include these limitations.

The examiner is reminded that in rejecting a claim for obviousness, he "should set forth in the Office action (A) The relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate, (B) The difference or differences in the claim over the applied references(s), (C) The proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter, and (D) an explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification." MPEP § 706.02(j).

The examiner responded to appellants argument by repeating his original argument and continuing as follows:

> "Applicant is reminded that repeating a verbose claim and then stating plainly that the references do not show all that is claimed <u>is a general allegation</u> in that specific elements of the claims and references are not addressed. [**Note that appellants indicated by boldface the limitations in each claim which are not disclosed by Carroll et al.**] If the applicant wishes to write 80 claims then the applicant should address each of the claim's and why the [*sic*] are patentable, merely stating 'the claimed elements aren't taught' is insufficient reason to withdraw the rejection. These claims are directed to means for modulation and demodulation. If the applicant attempts to read means plus function elements into these

claims then the applicant should specifically [*sic*] what structure is to be interpreted as the means, pointing to specific sections of the present specification for support." 01/15/04 Office Action, pp 23-24.

The examiner was either unable or chose not to cite particular passages in Carroll et al. pertaining to the particular claim limitations identified by appellants.

The examiner's position is contrary to case law:

"The legal concept of *prima facie* obviousness is a procedural tool of examination which applies broadly to all arts. It allocates who; as the burden of going forward with production of evidence in each step of the examination process. [case citations omitted] The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to suabmit evidence of; nonobviousness. MPEP § 2142.

The examiner has not established *prima facie* obviousness of claims 51-55.

CLAIM 56

Claim 56 reads as follows:

*56. A tag for use with a reader, **[1] the reader transmitting a bit-timing clock signal to the tag**, the tag comprising:*

a coil;

a capacitor;

a means for coupling the capacitor to the coil;

a means for driving the coil with a driving signal;

a means for generating the driving signal;

[2] a means for generating a bit-timing clock signal synchronized to the reader bit-timing clock signal;

[3] a means for embedding a sequence of bits to be communicated to a reader in the driving signal, the start of each bit being controlled by the bit-timing clock signal.

Carroll et al. does not teach the limitations of claim 56 shown in boldface, and there is no motivation for incorporating these limitations in Carroll et al.'s transponder 40.

Limitation [1]

Limitation [1] is not disclosed by Carroll et al. For details, please see discussion under the **ISSUE IV, CLAIM 70** heading.

The examiner argues that a preamble limitation is "generally not accorded any patentable weight where it merely recites the purpose of a process or the intended used of a structure and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone." 08/12/03 Office Action, p. 13.

Limitation [1] does not merely recite an intended use of the tag. One of the primary functions of a tag is to "read" the data transmitted by a reader. To do this, the structure of the tag must be tailored to the method used by the reader to transmit data. Thus, limitation [1] is clearly a limitation on the structure of the tag that cannot be ignored.

Limitation [2]

Carroll et al.'s controller 10 does not transmit a bit-timing clock signal to transponder 40 (see discussion under **ISSUE IV, CLAIM 70** heading). Consequently, there is no bit-timing clock signal

originating in controller 10 that could be used by transponder 40 to synchronize its own bit-timing clock. For additional discussion of this limitation, see **ISSUE IV, CLAIM 74,** ***Limitation [2].***

Carroll et al. does not teach Limitation [2].

Limitation [3]

Since the bit-timing clock signal specified by limitation [2] does not exist in Carroll et al.'s transponder 40, Carroll et al. obviously cannot disclose limitation [3] which requires this non-existent bit-timing clock signal.

Carroll et al. does not teach the boldface limitations of claim 56, and there is no motivation for incorporating these limitations in Carroll et al.'s transponder 40.

Prima facie obviousness of claim 56 has not been established.

The examiner argues that "Carroll is not cited for teaching each and every element as claimed" (08/12/03 Office Action, p. 24) and yet he cites no other references. The examiner argues that "applicant failed to appreciate the teachings of Carroll" (08/12/03 Office Action, p. 24). But pointing out that Carroll et al. does not disclose specified limitations in claims does not mean that applicants "failed to appreciate the teachings of Carroll." Finally, the examiner argues that "applicant ignored the application of Carroll as discussed in the OBVIOUSNESS rejection set forth in the Office Action" (08/12/03 Office Action, p. 24) but applicants are unable to find any discussion whatsoever of claim 56 and its limitations in the "obviousness" portion of the office action relating to Carroll et al. See 08/12/03 Office Action, pp. 7-8.

CLAIM 57

Claim 57 reads as follows:

57. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal to have a first phase when a "0" bit is being transmitted and to have a second phase when a "1" bit is being transmitted.

Carroll et al. teach the use of Manchester coded PSK in transmitting data from transponder 40 (analogous to applicants' tag) to controller 10. Carroll et al., col. 20, lines 33-35. Manchester-coded PSK results in the driving signal having (1) a first phase during the first half of a bit period and a second phase during the second half of a bit period when a "0" is transmitted and (2) the second phase during the first half of a bit period and the first phase during the second half of a bit period when a "1" is transmitted. Manchester-coded PSK is not a teaching of applicants' claim-57 limitation.

Manchester-coded PSK has some very desirable properties, and a person skilled in the art would not be motivated by knowledge generally available to one of ordinary skill in the art to change Carroll et al.'s modulation technique to the one specified in applicants' claim 57.

Carroll et al. does not teach the claim-57 limitation, and there is no motivation for changing Carroll et al.'s preferred modulation technique to the one specified in claim 57.

Prima facie obviousness of claim 57 has not been established.

The examiner argues that the claim language does not require "the phase be constant for the entire bit period." 08/12/03 Office Action, p. 25.

The examiner wants to interpret "a means for causing the phase of the driving signal to have a first phase when a "0" bit is being transmitted" as meaning "a means for causing the phase of the driving signal to have a first phase FOR AT LEAST A PORTION OF THE TIME when a "0" bit is being transmitted." But the words "FOR AT LEAST A PORTION OF THE TIME" do not appear in the claim.

Would the examiner also argue that the statement "the horn sounds when the horn button is being pushed" actually means "the horn sounds FOR AT LEAST A PORTION OF THE TIME when the horn button is being pushed"? More likely, the latter would be attributed to a malfunctioning horn circuit.

The language <u>does</u> require the phase of the driving signal to be a constant during the entire bit period and to be equal to a "first phase" when a "0" bit is being transmitted and to be equal to a "second phase" when a "1" bit is being transmitted. This interpretation of "phase" is consistent with the definition "an additive constant in the argument of a trigonometric function." McGraw-Hill Dictionary of Scientific and Technical Terms, Fourth Edition, McGraw-Hill, Inc., New York, N.Y. (1989).

In his most recent office action, the examiner insists that appellants' interpretation of the claim language is incorrect. The examiner makes the following argument.

> "The claim require [*sic*] a first phase for a "0" and a second phase for a "1". Here again the applicant is attempting to further limit the claims by unfairly "interpreting" limitations into the claims, which simply are not present. The applicant argues that the examiner's interpretation of the claim is incorrect because "for at least a portion of the time" does not exist in the claim. The claims do not preclude such an interpretation by including a

limitation such as "for the entire bit period" and since the claim is construed in the open language "comprising", it is well held that the claimed limitation need only exist once in the prior art to be taught by the references. 01/15/04 Office Action, p. 25.

The plain meaning of the claim is that the phase of the driving signal has a first phase when a "0" is being transmitted and a second phase when a "1" is being transmitted, and the plain meaning is what counts during examination. *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). The examiner may not import into the claim a limitation not present in the claim (such as "for at least a portion of the time").

"Comprising" is a term of art used in claim language which means that the named elements are essential, but other elements may be added and still form a construct within the scope of the claim. *Genentech, Inc. v. Chiron Corp.*, 112 F.3d 495, 501, 42 USPQ2d 1608, 1613 (Fed. Cir. 1997). The use of "comprising" does not give license to the examiner to add additional limitations to a particular claim element.

CLAIM 58

Claim 58 reads as follows:

58. The tag of claim 56 wherein the means for embedding a sequence of bits comprises: a means for modulating the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 58.

Carroll et al.'s controller 10 transmits data by changing the frequency of the driving signal. Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al., col. 3, lines 45-62. This is not the same as generating "a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted" and then using this "periodic signal" to modulate the driving signal.

Carroll et al. does not teach the claim-58 limitation, and there is no motivation for changing Carroll et al.'s preferred modulation technique to the one specified in claim 58.

Prima facie obviousness of claim 58 has not been established.

Rather than responding to appellants' arguments concerning the patentability of this claim, the examiner suggests that his arguments with respect to claim 57 are also applicable to claim 58. 01/15/04 Office Action, pp. 24. However, this is not true. Claim 57 has to do with causing the "driving signal" to have specific phase values depending on which bit value is being transmitted while claim 58 has to do with causing a "periodic signal" to have specific phase values depending on which bit value is being transmitted and then modulating the "driving signal" with this "periodic signal". Thus, the modulation technique prescribed in claim 58 is very different from the Manchester-encoded PSK and FSK techniques disclosed by Carroll et al. Please see discussion under the **CLAIM** 7 heading which argues the patentability of the same limitation in connection with a reader.

CLAIM 59

Claim 59 reads as follows:

59. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 59.

Carroll et al.'s controller 10 transmits data by changing the frequency of the driving signal. Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al., col. 3, lines 45-62. This is not the same as generating "a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted" and then using this "periodic signal" to amplitude modulate the driving signal.

Carroll et al. does not teach the claim-59 limitation, and there is no motivation for changing Carroll et al.'s preferred modulation technique to the one specified in claim 59.

Prima facie obviousness of claim 59 has not been established.

Rather than responding to appellants' arguments concerning the patentability of this claim, the examiner suggests that his arguments with respect to claim 57 are also applicable to claim 59. 01/15/04 Office Action, pp. 24. However, this is not true. Claim 57 has to do with causing the "driving signal" to have specific phase values depending on which bit value is being transmitted while claim 59 has to do with causing a "periodic signal" to have specific phase values depending on which bit value is being transmitted and then amplitude modulating the "driving signal" with this

"periodic signal". Thus, the modulation technique prescribed in claim 59 is very different from the Manchester-encoded PSK and FSK techniques disclosed by Carroll et al. Please see discussion under the **CLAIM 8** heading which argues the patentability of the same limitation in connection with a reader.

CLAIM 60

Claim 60 reads as follows:

60. The tag of claim 56 wherein the means for embedding a sequence of bits comprises: a means for modulating the phase of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 60.

Carroll et al.'s controller 10 transmits data by changing the frequency of the driving signal. Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al., col. 3, lines 45-62. This is not the same as generating "a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted" and then using this "periodic signal" to phase modulate the driving signal.

Carroll et al. does not teach the claim-60 limitation, and there is no motivation for changing Carroll et al.'s preferred modulation technique to the one specified in claim 60.

Prima facie obviousness of claim 60 has not been established.

Rather than responding to appellants' arguments concerning the patentability of this claim, the examiner suggests that his arguments with respect to claim 57 are also applicable to claim 60. 01/15/04 Office Action, pp. 24. However, this is not true. Claim 57 has to do with causing the "driving signal" to have specific phase values depending on which bit value is being transmitted while claim 60 has to do with causing a "periodic signal" to have specific phase values depending on which bit value is being transmitted and then phase modulating the "driving signal" with this "periodic signal". Thus, the modulation technique prescribed in claim 60 is very different from the Manchester-encoded PSK and FSK techniques disclosed by Carroll et al. Please see discussion under the **CLAIM 9** heading which argues the patentability of the same limitation in connection with a reader.

CLAIM 62

Claim 62 reads as follows:

62. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 62.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as generating "a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted" and then modulating the driving signal with this periodic signal.

Carroll et al. does not teach the limitation of claim 62, and consequently, prima facie obviousness of claim 62 has not been established.

Carroll et al. does not teach the claim-62 limitation, and there is no motivation for changing Carroll et al.'s preferred modulation technique to the one specified in claim 62.

Prima facie obviousness of claim 62 has not been established.

The examiner argued in the 08/12/03 Office Action that "[c]laim 62 for example modulates the driving signal with a first frequency to represent a "0" and modulates with a second frequency to represent a "1", this is the definition of FSK which is shown by Carroll." 08/12/03 Office Action, p. 25.

Appellants responded as follows.

What the examiner seems to be saying is that the claim-62 and Carroll et al.'s modulation techniques are simply different types of FSK and the differences can be ignored. The differences are substantial and cannot be ignored. All of the words in the claim must be considered:

> **"To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). All words in a claim must be considered in judging the patentability of that claim against the prior art. *In re Wilson*, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970)." MPEP § 2143.03.**

The examiner responded to the above by repeating his 08/12/03 argument and adding that "the applicant argues that all the words in the claim must be considered yet fails to point to any specific word(s) that the applicant believes were ignored by the examiner. 01/15/04 Office Action, p. 25.

To show how the examiner is misinterpreting claim 62, we reproduce the examiners interpretation of the claim language and the actual claim language below with the words ignored by the examiner shown by strikethroughs.

examiner's interpretation - "claim 62 for example modulates the driving signal with a first frequency to represent a "0" and modulates with a second frequency to represent a "1"

actual claim 62 limitation - *a means for modulating the driving signal with ~~a periodic signal having~~ a first frequency when a "0" bit is being transmitted and ~~having~~ a second frequency when a "1" bit is being transmitted.*

The examiner has completely changed the limitation by ignoring the presence of "periodic signal" in the claim.

This claim involves both a "driving signal" and a "periodic signal", a type of limitation wherein the second modulates the first. Please see discussion under the **CLAIM 11** heading which argues the patentability of the same limitation in connection with a reader.

CLAIM 63

Claim 63 reads as follows:

63. The tag of claim 56 wherein the means for embedding a sequence of bits comprises: a means for modulating the amplitude of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 63.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as generating "a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted" and then amplitude modulating the driving signal with this periodic signal.

Carroll et al. does not teach the claim-63 limitation, and there is no motivation for changing Carroll et al.'s preferred modulation technique to the one specified in claim 63.

Prima facie obviousness of claim 63 has not been established.

The examiner argued in the 08/12/03 Office Action that "[c]laim 62 for example modulates the driving signal with a first frequency to represent a "0" and modulates with a second frequency

to represent a "1", this is the definition of FSK which is shown by Carroll." 08/12/03 Office Action, p. 25.

Appellants responded as follows.

What the examiner seems to be saying is that the claim-62 and Carroll et al.'s modulation techniques are simply different types of FSK and the differences can be ignored. The differences are substantial and cannot be ignored. All of the words in the claim must be considered:

> **"To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). All words in a claim must be considered in judging the patentability of that claim against the prior art. *In re Wilson*, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970)." MPEP § 2143.03.**

The examiner responded to the above by repeating his 08/12/03 argument and adding that "the applicant argues that all the words in the claim must be considered yet fails to point to any specific word(s) that the applicant believes were ignored by the examiner. 01/15/04 Office Action, p. 25.

The examiner did not provide an interpretation of claim 63 (as he did for claim 62) but indicated that claims 62-64 were all claiming the FSK technique disclosed by Carroll et al. Since the examiner seems to feel that he has captured the essence of claims 62-64 in his claim-62 interpretation, we will compare the examiner's interpretation of the claim-62 language with the actual claim-63 language with the words ignored by the examiner shown by strikethroughs.

examiner's claim-62 interpretation - "claim 62 for example modulates the driving signal with a first frequency to represent a "0" and modulates with a second frequency to represent a "1"

claim-63 limitation - *a means for modulating the amplitude of the driving signal with ~~a periodic signal having~~ a first frequency when a "0" bit is being transmitted and ~~having~~ a second frequency when a "1" bit is being transmitted.*

As in the case of claim 62, the claim-63 limitation is completely changed by ignoring the presence of "periodic signal" in the claim.

This claim involves both a "driving signal" and a "periodic signal", a type of limitation wherein the second modulates the first. Please see discussion under the **CLAIM 12** heading which argues the patentability of the same limitation in connection with a reader.

CLAIM 64

Claim 64 reads as follows:

64. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 64.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to

send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as generating "a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted" and then phase modulating the driving signal with this periodic signal.

Carroll et al. does not teach the claim-64 limitation, and there is no motivation for changing Carroll et al.'s preferred modulation technique to the one specified in claim 64.

Prima facie obviousness of claim 64 has not been established.

The examiner argued in the 08/12/03 Office Action that "[c]laim 62 for example modulates the driving signal with a first frequency to represent a "0" and modulates with a second frequency to represent a "1", this is the definition of FSK which is shown by Carroll." 08/12/03 Office Action, p. 25. This argument would also seem to apply to claim 64. What the examiner seems to be saying is that the claim-62 (or claim-64) and Carroll et al.'s modulation techniques are simply different types of FSK and the differences can be ignored. The differences are substantial and cannot be ignored. All of the words in the claim must be considered:

> **"To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). All words in a claim must be considered in judging the patentability of that claim against the prior art. *In re Wilson*, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970)." MPEP § 2143.03.**

The examiner responded to the above by repeating his 08/12/03 argument and adding that "the applicant argues that all the words in the claim must be considered yet fails to point to any specific word(s) that the applicant believes were ignored by the examiner. 01/15/04 Office Action, p. 25.

The examiner did not provide an interpretation of claim 64 (as he did for claim 62) but indicated that claims 62-64 were all claiming the FSK technique disclosed by Carroll et al. Since the examiner seems to feel that he has captured the essence of claims 62-64 in his claim-62 interpretation, we will compare the examiner's interpretation of the claim-62 language with the actual claim-64 language with the words ignored by the examiner shown by strikethroughs.

examiner's claim-62 interpretation - "claim 62 for example modulates the driving signal with a first frequency to represent a "0" and modulates with a second frequency to represent a "1"

claim-64 limitation - *a means for modulating the phase of the driving signal with ~~a periodic signal having~~ a first frequency when a "0" bit is being transmitted and ~~having~~ a second frequency when a "1" bit is being transmitted.*

As in the case of claim 62, the claim-64 limitation is completely changed by ignoring the presence of "periodic signal" in the claim.

This claim involves both a "driving signal" and a "periodic signal", a type of limitation wherein the second modulates the first. Please see discussion under the **CLAIM 13** heading which argues the patentability of the same limitation in connection with a reader.

VIII. WHETHER CLAIMS 14-17, 61, AND 64-68 ARE UNPATENTABLE UNDER 35 U.S.C. § 103(A) IN VIEW OF CARROLL ET AL. (U.S. 5,517,194) AND MCFARLANE (U.S. 3,223,779).

CLAIM 14

Claim 14 reads as follows:

14. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal (1) to have a first phase and a first frequency when a "00" bit pair is being transmitted, (2) to have a first phase and a second frequency when a "01" bit pair is being transmitted, (3) to have a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) to have a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-15 limitation has to do with applying FSK/PSK modulation to the PHASE of a driving signal. Thus, McFarlane does not teach the limitation of claim 15.

The examiner does not accept appellants' assertion that (1) a means for causing a driving signal to have one of two frequency values and one of two phase values (McFarlane) is different than (2) causing the PHASE of driving signal to have one of two frequency values and one of two phase values (claim 14). To make the difference more obvious, we provide below the mathematical foundation of the assertion. *See The Communications Handbook*, CRC Press, Inc., Boca Raton, FL (1997), pp 9-12.

The starting point for a textbook discussion of modulation techniques wherein data is embedded in a carrier is the equation

$$s(t) = A\cos(2\pi f_c t + \theta)$$

which specifies that a carrier signal *s(t)* has an amplitude A, a frequency f_c, and a phase θ. Data can be embedded in the carrier signal by varying or modulating in accordance with the data one or more of the quantities that define the carrier signal, i.e. A, f_c, and θ. One can achieve even greater flexibility in choosing a modulation technique by specifying that θ is a sinusoid,

$$\theta = \Delta\theta \cos 2\pi f_m t + \theta_m$$

in which case the equation for *s(t)* becomes:

$$s(t) = A\cos(2\pi f_c t + \Delta\theta \cos 2\pi f_m t + \theta_m)$$

where $\Delta\theta$ is the maximum deviation of the frequency-modulated phase, f_m is the frequency of the frequency-modulated phase, and θ_m is the phase of the frequency-modulated phase. Data can now be embedded in the carrier signal by varying or modulating in accordance with the data one or more of the quantities A, f_c, f_m, and θ_m.

When claim 14 states that the "phase" of the driving signal has specified frequency and phase values, the specified frequency and phase values correspond to f_m (the frequency of the frequency-modulated phase), and θ_m (the phase of the frequency-modulated phase).

When McFarlane discloses a driving signal having a frequency of either f_1 or f_2 and one or the other of two phases, the frequencies and phases correspond to , the frequency f_c and the phase θ in the first equation above. Obviously, McFarlane's modulation technique is not the same as the one claimed in claim 14.

Even if the substitution of McFarlane's FSK/PSK communication circuitry for Carroll et al.'s FSK circuitry would result in a reader with the limitations of claim 14 (which it would NOT), there is no motivation for such a modification.

Carroll et al. utilize a simple FSK technique for communicating commands from controller 10 to transponder 40 where the controller 10 is constructed around a commercially-available microcomputer chip. Carroll et al., col. 5, line 64 - col. 6, line 16. The extraction of data from the received signal by transponder 40 is accomplished by a simple circuit consisting of an oscillator, an up/down counter, and logic circuits. Carroll et al., col. 18, lines 44-57.

McFarlane discloses a combined FSK/PSK communication technique which involves at the transmit end two frequency multipliers, two phase shifters, logic circuitry, and an analog signal combiner. McFarlane discloses data extraction circuitry at the receive end consisting of two filters, four frequency multipliers, four frequency dividers, two phase detectors, and associated logic circuitry. McFarlane, Fig. 1.

There is no motivation for a person skilled in the art to complicate the Carroll et al. invention by substituting a McFarlane's combined FSK/PSK modulation technique for Carroll et al.'s simple and straightforward FSK technique.

The examiner argues that "it would have been obvious . . . to have used both FSK and PSK simultaneously in the Carroll [*sic*] in order to increase the bandwidth of the system." 08/12/03 Office Action, p. 10. The object in designing communication systems is usually to use less bandwidth to communicate at a certain data rate. And Carroll et al.'s PSK approach is much more efficient in the use of bandwidth than is McFarlane's FSK/PSK approach. *The Communications Handbook*, CRC Press, Inc., Boca Raton, FL (1997), Fig. 19.1. Neither the examiner nor the

references provide a reasonable motivation for a person skilled in the art to incorporate McFarlane's FSK/PSK communication technique in Carroll et al.'s invention.

The references do not disclose the claim-14 limitation nor do the references provide motivation for making a changes in Carroll et al.'s controller 10 and transponder 40 to accomodate the FSK/PSK modulation techniques of McFarlane.

The examiner has not established *prima facie* obviousness of applicants' claim-14 invention.

CLAIM 15

Claim 15 reads as follows:

15. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-15 limitation has to do with applying FSK/PSK modulation to a periodic signal and then using this modulated periodic signal to modulate the driving signal. Thus, McFarlane does not teach the limitation of claim 15.

The references do not disclose the claim-15 limitation nor do the references provide motivation for making changes in Carroll et al.'s controller 10 and transponder 40 to accomodate the FSK/PSK modulation techniques of McFarlane. Please see discussion under the **CLAIM 14** heading for additional details.

Claim 15 involves the modulation of the "driving signal" by a "periodic signal", a limitation not disclosed by either of the references. The examiner consistently fails to recognize this difference in his comparison of the references with appellants' claims that include this limitation. Please see the discussion under the **ISSUE VII, CLAIM 7** heading for an example of the examiner's analysis of such claims.

The examiner has not established *prima facie* obviousness of applicants' claim-15 invention.

CLAIM 16

Claim 16 reads as follows:

16. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-16

limitation has to do with applying FSK/PSK modulation to a periodic signal and then using this modulated periodic signal to amplitude modulate the driving signal. Thus, McFarlane does not teach the limitation of claim 16.

The references do not disclose the claim-16 limitation nor do the references provide motivation for making a changes in Carroll et al.'s controller 10 and transponder 40 to accomodate the FSK/PSK modulation techniques of McFarlane. Please see discussion under the **CLAIM 14** heading for additional details.

Claim 16 involves the modulation of the "driving signal" by a "periodic signal", a limitation not disclosed by either of the references. The examiner consistently fails to recognize this difference in his comparison of the references with appellants' claims that include this limitation. Please see the discussion under the **ISSUE VI, CLAIM 7** heading for an example of the examiner's analysis of such claims.

The examiner has not established *prima facie* obviousness of applicants' claim-16 invention.

CLAIM 17

Claim 17 reads as follows:

17. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-17 limitation has to do with applying FSK/PSK modulation to a periodic signal and then using this modulated periodic signal to phase modulate the driving signal. Thus, McFarlane does not teach the limitation of claim 17.

The references do not disclose the claim-17 limitation nor do the references provide motivation for making a changes in Carroll et al.'s controller 10 and transponder 40 to accomodate the FSK/PSK modulation techniques of McFarlane. Please see discussion under the **CLAIM 14** heading for additional details.

Claim 17 involves the modulation of the "driving signal" by a "periodic signal", a limitation not disclosed by either of the references. The examiner consistently fails to recognize this difference in his comparison of the references with appellants' claims that include this limitation. Please see the discussion under the **ISSUE VII, CLAIM 7** heading for an example of the examiner's analysis of such claims.

The examiner has not established *prima facie* obviousness of applicants' claim-17 invention.

CLAIM 61

Claim 61 reads as follows:

61. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal to have a first frequency when a "0" bit is being transmitted and to have a second frequency when a "1" bit is being transmitted.

Neither Carroll et al. nor McFarlane disclose a modulation technique wherein the PHASE of the driving signal has a first frequency when a "0" bit is being transmitted and a second frequency when a "1" bit is being transmitted. This is NOT the same as a modulation technique wherein the DRIVING SIGNAL has a first frequency when a "0" bit is being transmitted and a second frequency when a "1" bit is being transmitted. For information relating to the modulation of the PHASE of the driving signal in the context of a reader, please see discussion under the **CLAIM 14** heading.

Carroll et al. teach the use of Manchester coded PSK in transmitting data from transponder 40 (analogous to applicants' tag) to controller 10. Carroll et al., col. 20, lines 33-35. Manchester-coded PSK results in the driving signal having (1) a first phase during the first half of a bit period and a second phase during the second half of a bit period when a "0" is transmitted and (2) the second phase during the first half of a bit period and the first phase during the second half of a bit period when a "1" is transmitted.

Manchester-coded PSK has some very desirable properties, and a person skilled in the art would not be motivated by knowledge generally available to one of ordinary skill in the art to change Carroll et al.'s modulation technique to the one specified in applicants' claim 61.

Neither of the references teaches the claim-61 limitation, and there is no motivation for changing Carroll et al.'s preferred modulation technique to the one specified in claim 61. The examiner argues that "it would have been obvious . . . to have used both FSK and PSK simultaneously in the Carroll [*sic*] in order to increase the bandwidth of the system." 08/12/03 Office Action, p. 10. The object in designing communication systems is usually to use less bandwidth to communicate at a certain data rate. And Carroll et al.'s PSK approach is much more

efficient in the use of bandwidth than is McFarlane's FSK/PSK approach. *The Communications Handbook*, CRC Press, Inc., Boca Raton, FL (1997), Fig. 19.1. Neither the examiner nor the references provide a reasonable motivation for a person skilled in the art to incorporate McFarlane's FSK/PSK communication technique in Carroll et al.'s invention.

The references do not disclose the claim-61 limitation nor do the references provide motivation for making a changes in Carroll et al.'s controller 10 and transponder 40 to accomodate the FSK/PSK modulation techniques of McFarlane.

The examiner has not established *prima facie* obviousness of applicants' claim-61 invention.

CLAIM 64

Claim 64 reads as follows:

64. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

Neither Carroll et al. nor McFarlane disclose a modulation technique wherein the PHASE of the driving signal is modulated by a PERIODIC signal having a first frequency when a "0" bit is being transmitted and a second frequency when a "1" bit is being transmitted. This is NOT the same as a modulation technique wherein the DRIVING SIGNAL has a first frequency when a "0" bit is being transmitted and a second frequency when a "1" bit is being transmitted. For information

relating to the modulation of the PHASE of the driving signal in the context of a reader, please see discussion under the **CLAIM 14** heading.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 64.

Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29.

Carroll et al.'s transponder 40 transmits data by Manchester-coded PSK whereby a driving signal has (1) a first phase during the first half of a bit period and a second phase during the second half of a bit period when a "0" is transmitted and (2) the second phase during the first half of a bit period and the first phase during the second half of a bit period when a "1" is transmitted. Carroll et al., col. 20, lines 33-35.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34.

Applicants' claim-64 limitation has to do with applying FSK modulation to a periodic signal and then using this modulated periodic signal to phase modulate the driving signal. Thus, neither Carroll et al. nor McFarlane teaches the limitation of claim 64.

Even if the substitution of McFarlane's FSK/PSK communication circuitry for Carroll et al.'s PSK circuitry would result in a transponder with the limitations of claim 64 (which it would NOT), there is no motivation for making such a modification.

The examiner argues that "it would have been obvious . . . to have used both FSK and PSK simultaneously in the Carroll [*sic*] in order to increase the bandwidth of the system." 08/12/03 Office Action, p. 10. The object in designing communication systems is usually to use less bandwidth to communicate at a certain data rate. And Carroll et al.'s PSK approach is much more efficient in the use of bandwidth than is McFarlane's FSK/PSK approach. *The Communications Handbook*, CRC Press, Inc., Boca Raton, FL (1997), Fig. 19.1. Neither the examiner nor the references provide a reasonable motivation for a person skilled in the art to incorporate McFarlane's FSK/PSK communication technique in Carroll et al.'s invention.

The references do not disclose the claim-64 limitation nor do the references provide motivation for making a change in Carroll et al.'s transponder 40 modulation technique.

The examiner has not established *prima facie* obviousness of applicants' claim-64 invention.

CLAIM 65

Claim 65 reads as follows:

65. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal (1) to have a first phase and a first frequency when a "00" bit pair is being transmitted, (2) to have a first phase and a second frequency when a "01" bit pair is being transmitted, (3) to have a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) to have a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-65 limitation has to do with applying FSK/PSK modulation to the PHASE of a driving signal. (For information relating to the modulation of the PHASE of the driving signal in the context of a reader, please see discussion under the **CLAIM 14** heading.) Thus, McFarlane does not teach the limitation of claim 15.

Carroll et al. utilize a simple PSK technique for communicating data from transponder 40 to controller 10 where the controller 10 is constructed around a commercially-available microcomputer chip. Carroll et al., col. 5, line 64 - col. 6, line 16. The extraction of data from the received signal by transponder 40 is accomplished by the microcomputer chip. Carroll et al., col. 7, lines 12-16. McFarlane discloses a combined FSK/PSK communication technique which involves at the transmit end two frequency multipliers, two phase shifters, logic circuitry, and an analog signal combiner. McFarlane discloses data extraction circuitry at the receive end consisting of two filters, four frequency multipliers, four frequency dividers, two phase detectors, and associated logic circuitry. McFarlane, Fig. 1.

Even if the substitution of McFarlane's FSK/PSK communication circuitry for Carroll et al.'s PSK circuitry would result in a transponder with the limitations of claim 65 (which it would NOT), there is no motivation for making such a modification.

The examiner argues that "it would have been obvious . . . to have used both FSK and PSK simultaneously in the Carroll [*sic*] in order to increase the bandwidth of the system." 01/15/04 Office Action, p. 8. The object in designing communication systems is usually to use less bandwidth to communicate at a certain data rate. And Carroll et al.'s PSK approach is much more efficient in

the use of bandwidth than is McFarlane's FSK/PSK approach. *The Communications Handbook*, CRÇ Press, Inc., Boca Raton, FL (1997), Fig. 19.1. Neither the examiner nor the references provide a reasonable motivation for a person skilled in the art to incorporate McFarlane's FSK/PSK communication technique in Carroll et al.'s invention.

The references do not disclose the claim-65 limitation nor do the references provide motivation for making a change in Carroll et al.'s transponder 40 modulation technique.

The examiner has not established *prima facie* obviousness of applicants' claim-65 invention.

CLAIM 66

Claim 66 reads as follows:

66. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-66 limitation has to do with applying FSK/PSK modulation to a periodic signal and then using this modulated periodic signal to modulate the driving signal. Thus, McFarlane does not teach the limitation of claim 66.

The references do not disclose the claim-66 limitation nor do the references provide motivation for making a change in Carroll et al.'s controller 10 modulation technique. Please see discussion under the **CLAIM 65** heading for additional details.

Claim 66 involves the modulation of the "driving signal" by a "periodic signal", a limitation not disclosed by either of the references. The examiner consistently fails to recognize this difference in his comparison of the references with appellants' claims that include this limitation. Please see the discussion under the **ISSUE VII, CLAIM 7** heading for an example of the examiner's analysis of such claims.

The examiner has not established *prima facie* obviousness of applicants' claim-66 invention.

CLAIM 67

Claim 67 reads as follows:

67. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-67 limitation has to do with applying FSK/PSK modulation to a periodic signal and then using this

modulated periodic signal to amplitude modulate the driving signal. Thus, McFarlane does not teach the limitation of claim 67.

The references do not disclose the claim-67 limitation nor do the references provide motivation for making a change in Carroll et al.'s transponder 40 modulation technique. Please see discussion under the **CLAIM 65** heading for additional details.

Claim 67 involves the modulation of the "driving signal" by a "periodic signal", a limitation not disclosed by either of the references. The examiner consistently fails to recognize this difference in his comparison of the references with appellants' claims that include this limitation. Please see the discussion under the **ISSUE VII, CLAIM 7** heading for an example of the examiner's analysis of such claims.

The examiner has not established *prima facie* obviousness of applicants' claim-67 invention.

CLAIM 68

Claim 68 reads as follows:

68. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-68 limitation has to do with applying FSK/PSK modulation to a periodic signal and then using this modulated periodic signal to phase modulate the driving signal. Thus, McFarlane does not teach the limitation of claim 68. . (For information relating to the modulation of the PHASE of the driving signal in the context of a reader, please see discussion under the **CLAIM 14** heading.)

The references do not disclose the claim-68 limitation nor do the references provide motivation for making a change in Carroll et al.'s transponder 40 modulation technique. Please see discussion under the **CLAIM 65** heading for additional details.

Claim 68 involves the modulation of the "driving signal" by a "periodic signal", a limitation not disclosed by either of the references. The examiner consistently fails to recognize this difference in his comparison of the references with appellants' claims that include this limitation. Please see the discussion under the **ISSUE VII, CLAIM 7** heading for an example of the examiner's analysis of such claims.

The examiner has not established *prima facie* obviousness of applicants' claim-68 invention.

APPENDIX

1. A reader for use with a tag that communicates data to the reader, the reader comprising:

a transformer having a plurality of windings, each winding having first and second terminals;

a coil driver having first and second output terminals;

two capacitors, each capacitor having first and second terminals, the first and second output terminals of the coil driver being connected to the first terminals of the capacitors, the second terminals of the capacitors being connected to the first and second terminals of a winding of the transformer;

a coil having first and second terminals connected respectively to the first and second end terminals of a winding of the transformer;

a data extractor for extracting data from the signal induced in the coil, the data extractor having first and second terminals connected respectively to first and second terminals of a winding of the transformer.

2. The reader of claim 1 wherein the transformer has a first winding and a second winding, the capacitors being connected to the first winding, the coil being connected to the second winding, and the data extractor being connected to the first winding.

3. The reader of claim 1 wherein the transformer has a first winding and a second winding, the capacitors being connected to the first winding, the coil being connected to the second winding, and the data extractor being connected to the second winding.

4. The reader of claim 1 wherein the transformer has a first winding, a second winding, and a third winding, the capacitors being connected to the first winding, the coil being connected to

the second winding, and the data extractor being connected to the third winding.

5. A reader for use with a tag, the reader comprising:

a coil;

at least one capacitor;

a means for coupling the capacitor(s) to the coil;

a means for driving the coil through the capacitor(s) with a driving signal;

a means for generating the driving signal;

a means for embedding a bit-timing clock signal in the driving signal;

a means for embedding a sequence of bits to be communicated to a tag in the driving signal.

6. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal to have a first phase when a "0" bit is being transmitted and to have a second phase when a "1" bit is being transmitted.

7. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

8. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

9. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being

transmitted.

10. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal to have a first frequency when a "0" bit is being transmitted and to have a second frequency when a "1" bit is being transmitted.

11. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

12. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

13. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

14. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal (1) to have a first phase and a first frequency when a "00" bit pair is being transmitted, (2) to have a first phase and a second frequency when a "01" bit pair is being transmitted, (3) to have a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) to have a second phase and a second frequency when a "11" bit pair is being transmitted.

15. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

16. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

17. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

18. The reader of claim 5 wherein the bit-timing clock signal is used by the tag to control the start time of each bit transmitted to the reader, the reader further comprising:

a means for extracting data communicated by the tag from a coupling-means signal.

19. The reader of claim 18 wherein the tag transmits a first signal during a bit period

when a "0" bit is to be communicated and a second signal during a bit period when a "1" is to be communicated, the data-extracting means comprising:

a means for identifying the bit communicated by the tag during each bit period, the start of each bit period being determined by the bit-timing clock signal.

20. The reader of claim of 19 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the coupling-means signal;

a means for translating the weighted integration(s) into a bit value.

21. The reader of claim of 19 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the amplitude of the coupling-means signal;

a means for translating the weighted integration(s) into a bit value.

22. The reader of claim of 19 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the phase of the coupling-means signal;

a means for translating the weighted integration(s) into a bit value.

23. The reader of claim 19 wherein the first signal is a periodic signal with a first value for a predetermined signal parameter and the second signal is the periodic signal with a second value for the predetermined signal parameter, the predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the periodic signal, the bit-identifying means comprising:

a means for generating a first replica of the periodic signal with the first value for the predetermined signal parameter and a second replica of the periodic signal with the second value for

the predetermined signal parameter;

a means for multiplying the coupling-means signal by the first replica thereby obtaining a first product waveform and by the second replica thereby obtaining a second product waveform;

a means for integrating the first and second product waveforms for a bit period and translating the integration results into a bit value.

24. The reader of claim 19 wherein the first signal is a periodic signal with a first value for a first predetermined signal parameter and the second signal is the periodic signal with a second value for the first predetermined signal parameter, the first predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the periodic signal, the periodic signal modulating a second predetermined signal parameter of a carrier signal, the second predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the carrier signal, the bit-identifying means comprising:

a means for demodulating the second predetermined signal parameter of the coupling-means signal;

a means for generating a first replica of the periodic signal with the first value for the first predetermined signal parameter and a second replica of the periodic signal with the second value for the first predetermined signal parameter;

a means for multiplying the demodulated coupling-means signal by the first replica thereby obtaining a first product waveform and by the second replica thereby obtaining a second product waveform;

a means for integrating the first and second product waveforms for a bit period and translating the integration results into a bit value.

25. A reader for use with a tag that transmits a periodic signal having a first frequency when a "0" bit is to be communicated and a second frequency when a "1" bit is to be communicated, the reader comprising:

a means for receiving the tag signal;

a means for measuring the period of each cycle of the signal received from the tag during a bit period.

26. The reader of claim 25 further comprising:

a means for identifying the bit transmitted by the tag from the measurements of the period of each cycle of the signal received from the tag during a bit period.

27. The reader of claim 26 wherein the means for identifying the bit transmitted by the tag comprises:

a means for identifying the frequency of each cycle of the received signal, the frequency of a cycle being the first frequency if the absolute value of the difference between the period of the cycle and the period of the first-frequency signal is less than a first predetermined value, the frequency of a cycle being the second frequency if the absolute value of the difference between the period of the cycle and the period of the second-frequency signal is less than a second predetermined value;

a means for identifying the bit transmitted during a bit period from the frequencies of the cycles of the received signal, the bit being a "0" if the number of first-frequency cycles exceeds the number of second-frequency cycles in the bit period, the bit otherwise being a "1".

28. The reader of claim 26 wherein the means for identifying the bit transmitted by the tag comprises:

a means for identifying the frequency of each cycle of the received signal, the frequency of a cycle being the first frequency if the period of the cycle is greater than a first predetermined value and less than a second predetermined value, the frequency of a cycle being the second frequency if the period of the cycle is greater than a third predetermined value and less than a fourth predetermined value;

a means for identifying the bit transmitted during a bit period from the frequencies of the cycles of the received signal, the bit being a "0" if the number of first-frequency cycles exceeds the number of second-frequency cycles in the bit period, the bit otherwise being a "1".

29. The reader of claim 25 further comprising:

a means for identifying the beginning of a bit period, the beginning of a bit period being identified by a change greater than a predetermined value in the period of a cycle from one cycle to the next cycle.

30. The reader of claim 25 further comprising:

a means for identifying the frequency of each cycle of the received signal, the frequency of a cycle being the first frequency if the absolute value of the difference between the period of the cycle and the period of the first-frequency signal is less than a first predetermined value, the frequency of a cycle being the second frequency if the absolute value of the difference between the period of the cycle and the period of the second-frequency signal is less than a second predetermined value;

a means for identifying the beginning of a bit period, the beginning of a bit period being identified by a change in frequency from one cycle to the next.

31. The reader of claim 25 further comprising:

a means for identifying the frequency of each cycle of the received signal, the frequency of a cycle being the first frequency if the period of the cycle is greater than a first predetermined value and less than a second predetermined value, the frequency of a cycle being the second frequency if the period of the cycle is greater than a third predetermined value and less than a fourth predetermined value;

a means for identifying the beginning of a bit period, the beginning of a bit period being identified by a change in frequency from one cycle to the next.

32. A reader for use with a tag that transmits a data sequence to the reader by repeating a message a plurality of times, the message comprising a preamble , a tag data group of T bits, and an error-detecting group of E bits, the preamble consisting of a sync sequence of S bits, the tag data group and the error-detecting group possibly including false-sync sequences, the reader comprising:

a means for receiving the data sequence transmitted by the tag;

a means for detecting each sync sequence in the received data sequence;

a means for identifying the preamble;

a means for extracting the tag data group from the received data sequence utilizing the identification of the preamble.

33. The reader of claim 32 wherein the preamble identifying means comprises:

a means for detecting errors in the T + E bits following each detected sync sequence assuming that the sequence in question is the preamble, the presence of errors indicating that the sync sequence in question is a false-sync sequence, the absence of errors indicating that the sequence is, in fact, the preamble.

34. The reader of claim 33 wherein the sync sequence detecting means comprises:

a memory for storing (S+T+E) received data bits;

a means for determining whether the oldest S bits in memory is a sync sequence;

a means for replacing the oldest bit in memory with the next received bit after the memory has been filled with received bits;

a control means for causing the determining means and the replacing means to operate alternately after the memory is filled with received bits.

35. The reader of claim 33 wherein the sync sequence detecting means comprises:

a memory for storing (S+T+E) received data bits;

a first means for determining whether the newest S bits in memory is a sync sequence;

a second means for determining whether the oldest S bits in memory is a sync sequence;

a means for replacing the oldest bit in memory with the next received bit after the memory has been filled with received bits;

a control means for causing the first determining means and the replacing means to operate alternately until a sync sequence is detected, the control means causing the second determining means and the replacing means to operate alternately if a detected sync sequence is determined to be a false-sync sequence.

36. A reader for use with a tag, the reader comprising:

a coil;

at least one capacitor;

a means for coupling the capacitor(s) to the coil;

a means for driving the coil through the capacitor(s) with a driving signal, the means consisting of four field-effect transistors connected in a bridge arrangement, two opposing junctions

being connected to a power supply, the driving signal being available at the remaining two opposing junctions, the current flow through the transistors being controlled by a control signal applied to the gate of each transistor;

a means for generating at least one control signal.

37. The reader of claim 36 wherein the bridge circuit comprises two series-connected P- and N-channel field effect transistors connected in parallel, the junction of the P devices and the junction of the N devices being connected to a voltage supply, the driving signal being available at the junctions of the P and N devices.

38. The reader of claim 37 further comprising:

a diode connected between gate and source of each transistor to protect the gates from voltage spikes;

a resistor in series with each gate of each transistor to suppress ringing in the gate circuit when the transistor is turned on.

39. The reader of claim 36 wherein the bridge circuit comprises four N-channel field effect transistors connected source to drain, source to source, drain to source, and drain to drain, the junction of the drains and the junction of the sources being connected to a voltage supply, the driving signal being available at the source-drain junctions.

40. The reader of claim 39 further comprising a two-winding transformer associated with each transistor, a control signal being fed into one winding of a transformer, the other winding being connected between gate and source electrodes of the associated transistor.

41. A tag for use with a reader, the tag comprising:

a transformer having a plurality of windings, each winding having first and second terminals;

a coil having first and second terminals connected respectively to the first and second terminals of a winding of the transformer;

a capacitor having first and second terminals connected respectively to the first and second terminals of a winding of the transformer;

a coil driver having first and second terminals connected respectively to the first and second terminals of a winding of the transformer;

a data extractor for extracting the data from the signal induced in the coil, the data extractor having first and second terminals connected to the first and second terminals of a winding of the transformer;

a power extractor for extracting power from the signal induced in the coil to operate the tag, the power extractor having first and second terminals connected respectively to the first and second terminals of a winding of the transformer.

42. The tag of claim 41 wherein the transformer has a first winding and a second winding, the capacitor, the coil driver, the data extractor, and the power extractor being connected to the first winding, the coil being connected to the second winding.

43. The tag of claim 41 wherein the transformer has a first winding and a second winding, the capacitor and the coil driver being connected to the first winding, the coil, the data extractor, and the power extractor being connected to the second winding.

44. The tag of claim 41 wherein the transformer has a first winding, a second winding, and a third winding, the capacitor and the coil driver being connected to the first winding, the data extractor and the power extractor being connected to the second winding, and the coil being connected to the third winding.

45. The tag of claim 41 wherein the transformer has a first winding, a second winding, a third winding, and a fourth winding, the capacitor and the coil driver being connected to the first winding, the data extractor being connected to the second winding, the power extractor being connected to the third winding, and the coil being connected to the fourth winding.

46. The tag of claim 41 wherein the transformer has a first winding, a second winding, a third winding, a fourth winding, and a fifth winding, the capacitor being connected to the first winding, the coil driver being connected to the second winding, the data extractor being connected to the third winding, the power extractor being connected to the fourth winding, and the coil being connected to the fifth winding.

47. A tag for use with a reader, the reader communicating a sequence of bits to the tag by transmitting a first signal during a bit period when a "0" bit is to be communicated and a second signal during a bit period when a "1" is to be communicated, the reader embedding a bit-timing clock signal in the transmitted signals, the tag comprising:

a coil;

a capacitor;

a means for coupling the capacitor to the coil and coupling the coil to at least one other means, the signal(s) provided to the other means as a result of the coupling being called coupling-means signal(s), the combination of the coil, the capacitor, and the coupling means being called the resonating circuit;

a means for generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded in the transmitted signals;

a means for identifying the bit being transmitted during each bit period, the beginning and

ending of each bit period being indicated by the bit-timing clock signal.

48. The tag of claim of 47 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the coupling-means signal;

a means for translating the weighted integration(s) into a bit value.

49. The tag of claim of 47 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the amplitude of the coupling-means signal;

a means for translating the weighted integration(s) into a bit value.

50. The tag of claim of 47 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the phase of the coupling-means signal;

a means for translating the weighted integration(s) into a bit value.

51. The tag of claim 47 wherein the first signal is a periodic signal with a first value for a predetermined signal parameter and the second signal is the periodic signal with a second value for the predetermined signal parameter, the predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the periodic signal, the bit-identifying means comprising:

a means for generating a first replica of the periodic signal with the first value for the predetermined signal parameter and a second replica of the periodic signal with the second value for the predetermined signal parameter;

a means for multiplying the coupling-means signal by the first replica thereby obtaining a first product waveform and by the second replica thereby obtaining a second product waveform;

a means for integrating the first and second product waveforms for a bit period and translating the integration results into a bit value.

52. The tag of claim 47 wherein the first signal is a periodic signal with a first value for a first predetermined signal parameter and the second signal is the periodic signal with a second value for the first predetermined signal parameter, the first predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the periodic signal, the periodic signal modulating a second predetermined signal parameter of a carrier signal, the second predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the carrier signal, the bit-identifying means comprising:

a means for demodulating the second predetermined signal parameter of the coupling-means signal;

a means for generating a first replica of the periodic signal with the first value for the first predetermined signal parameter and a second replica of the periodic signal with the second value for the first predetermined signal parameter;

a means for multiplying the demodulated coupling-means signal by the first replica thereby obtaining a first product waveform and by the second replica thereby obtaining a second product waveform;

a means for integrating the first and second product waveforms for a bit period and translating the integration results into a bit value.

53. The tag of claim 47 wherein the bit-identifying means comprises:

a means for generating replicas of the first and second signals transmitted by the reader;

a means for obtaining the amplitude of a coupling-means signal as a function of time;

a means for multiplying the coupling-means signal amplitude by the replica of the first signal to obtain a first product signal and by the replica of the second signal to obtain a second product signal;

a means for integrating the first product signal over a bit period to obtain a first integration and integrating the second product signal over a bit period to obtain a second integration;

a means for translating the first and second integrations into a bit value.

54. The tag of claim 47 wherein the means for generating a bit-timing clock signal that indicates the start of each bit period comprises:

a means for generating a clock signal having a bit-start indicator during each bit period, the bit-start indicators being adjustable in time;

a means for recognizing the bit transition in the coupling-means signal from one bit to the next;

a means for adjusting the bit-start indicators until the bit-start indicators and the bit transitions in the coupling-means signal occur simultaneously.

55. The tag of claim 47 wherein the reader embeds a bit-timing clock signal in the transmitted signals by initially alternating the transmission of the first signal and the second signal, the means for generating a bit-timing clock signal that indicates the start of each bit period comprising:

a means for generating a clock signal having a bit-start indicator during each bit period, the bit-start indicators being adjustable in time;

a means for recognizing the bit transitions in the coupling-means signal resulting from the transitions from the first signal to the second signal and from the second signal to the first signal;

a means for adjusting the bit-start indicators until the bit-start indicators and the transitions in the coupling-means signal occur simultaneously.

56. A tag for use with a reader, the reader transmitting a bit-timing clock signal to the tag, the tag comprising:

a coil;

a capacitor;

a means for coupling the capacitor to the coil;

a means for driving the coil with a driving signal;

a means for generating the driving signal;

a means for generating a bit-timing clock signal synchronized to the reader bit-timing clock signal;

a means for embedding a sequence of bits to be communicated to a reader in the driving signal, the start of each bit being controlled by the bit-timing clock signal.

57. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal to have a first phase when a "0" bit is being transmitted and to have a second phase when a "1" bit is being transmitted.

58. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

59. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being

transmitted.

60. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

61. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal to have a first frequency when a "0" bit is being transmitted and to have a second frequency when a "1" bit is being transmitted.

62. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

63. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

64. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

65. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal (1) to have a first phase and a first

frequency when a "00" bit pair is being transmitted, (2) to have a first phase and a second frequency when a "01" bit pair is being transmitted, (3) to have a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) to have a second phase and a second frequency when a "11" bit pair is being transmitted.

66. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

67. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

68. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

69. The tag of claim 56 wherein the reader transmits the bit-timing clock signal to the tag by communicating a sequence of alternating "0" and "1" bits, a "0" bit being communicated by modulating the amplitude of the driving signal with a first periodic signal, a "1" bit being communicated by modulating the amplitude of the alternating field with a second periodic signal, the means for generating the clock signal that is synchronized to the bit-timing signal transmitted by the reader to the tag comprising:

a means for generating a clock signal having a bit-start indicator during each bit period, the bit-start indicators being adjustable in time;

a means for obtaining the amplitude of a coupling-means signal as a function of time;

a means for recognizing the transitions in the coupling-means signal amplitude at the time interfaces of the first and second periodic signals;

a means for adjusting the bit-start indicators until the bit-start indicators and the transitions in the coupling-means signal amplitude occur simultaneously.

70. A method for interrogating a tag comprising the steps:

generating an alternating magnetic field;

embedding a bit-timing clock signal in the alternating magnetic field;

embedding data to be communicated to a tag in the alternating magnetic field.

71. A method for interrogating a tag, the tag responding to an interrogation by transmitting a sequence of bits, the start of each bit being determined by a bit-timing clock signal generated by the tag and synchronized with a bit-timing clock signal originating with the interrogator, the method comprising the steps:

generating a bit-timing clock signal;

generating an alternating magnetic field in which the bit-timing clock signal is embedded;

extracting data transmitted by the tag utilizing the bit-timing clock signal.

72. A method of receiving a data sequence transmitted by a tag consisting of a message repeated a plurality of times, the message comprising a preamble, a tag data group of T bits, and an error-detecting group of E bits, the preamble consisting of a sync sequence of S bits, the tag data group and the error-detecting group possibly including false-sync sequences, the method comprising the steps:

receiving the data sequence transmitted by the tag;

detecting each sync sequence in the received data sequence;

identifying the preamble;

extracting the tag data group from the received data sequence utilizing the identification of the preamble.

73. A method for responding to an interrogation by a reader, the method utilizing a resonating circuit comprising at least one capacitor coupled to a coil, the method comprising the steps:

driving the resonating circuit with a driving signal;

maintaining the resonating circuit in resonance;

embedding the sequence of bits to be communicated to the reader in the driving signal.

74. A method for responding to the establishment of an alternating magnetic field by a reader, the reader embedding a bit-timing clock signal in the alternating magnetic field and communicating a sequence of bits by modulating the alternating magnetic field, the method comprising the steps:

deriving a signal from the alternating magnetic field;

generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded in the alternating magnetic field;

performing at least one weighted integration of the derived signal over a bit period using the bit-timing clock signal to identify the beginning and end of a bit period;

identifying the bit being transmitted during each bit period utilizing the weighted integration(s).

75. A method for responding to the establishment of an alternating magnetic field by a reader, a bit-timing signal being embedded in the alternating magnetic field by the reader, the method comprising the steps:

deriving a signal from the alternating magnetic field;

generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded by the reader in the alternating magnetic field;

generating an alternating magnetic field;

modulating the alternating field generated by the responder with a sequence of bits to be communicated to a reader, the start of each transmitted bit being governed by the bit-timing clock signal.

76. A method of communication between an interrogator and a responder, the method performed by the interrogator comprising the steps:

generating an alternating magnetic field;

embedding a bit-timing clock signal in the alternating magnetic field;

extracting data communicated by the responder from an alternating magnetic field generated

by the responder;

the method performed by the responder comprising the steps:

extracting the bit-timing clock signal from the alternating magnetic field generated by the interrogator;

generating a bit-timing clock signal that is synchronized to the bit-timing clock signal originating with the interrogator;

generating an alternating magnetic field;

embedding data to be communicated to the interrogator in the alternating magnetic field generated by the responder, the start of each bit being controlled by the bit-timing clock signal generated by the responder.

77. A method of communication between an interrogator and a responder, the method performed by the interrogator comprising the steps:

generating an alternating magnetic field;

embedding a bit-timing clock signal in the alternating magnetic field;

embedding data to be communicated to the responder in the alternating magnetic field;

the method performed by the responder comprising the steps:

extracting a bit-timing clock signal from the alternating magnetic field generated by the interrogator;

performing at least one weighted integration of a signal derived from the alternating magnetic field generated by the interrogator over a bit period using the bit-timing clock signal to identify the beginning and end of a bit period;

identifying the bit being transmitted during each bit period utilizing the weighted

integration(s).

78. An apparatus for practicing the method of claim 73.

79. An apparatus for practicing the method of claim 76.

80. An apparatus for practicing the method of claim 7.

ATTACHMENT I

spectral waveshape would produce an infinitely long time domain record. However, from a hardware cost or throughput standpoint, it is unreasonable to consider the implementing of an infinitely or extremely long FIR. Therefore, a realizable FIR would be defined in terms of a truncated Fourier series. For example, the Fourier transform of the "nearly ideal" $N = 101$ order low-pass filter has a $\sin(x)/x$ type impulse-response envelope. For a large value of N, the difference between the response of an infinitely long impulse response and its N-sample approximation is small. However, when N is small, large approximation errors can occur.

16.8.8.1 Optimal Modeling Techniques. Weighted Chebyshev polynomials have been successfully used to design FIRs. In this application, Chebyshev polynomials are combined so that their combined sum minimizes the maximum difference between an ideal and the realized frequency response (i.e., mini-max principle). Because of the nature of these polynomials, they produce a "rippled" magnitude frequency-response envelope of equal minima and maxima in the pass- and stopbands. As a result, this class of filters is often called an *equiripple* filter. Much is known about the synthesis process, which can be traced back to McClellan et al.[48] Based on these techniques, a number of software-based CAD tools have been developed to support FIR design.

16.8.9 Windows

Digital filters usually are expected to operate over long, constantly changing data records. An FIR, while being capable of offering this service, can only work with a limited number of samples at a time. A similar situation presents itself in the context of a discrete Fourier transform. The quality of the produced spectrum is a function of the number of transformed samples. Ideally, an infinitely long impulse response would be defined by an ideal filter. A *uniform window* of length T will pass N contiguous samples of data. The windowing effect may be modeled as a multiplicative switch that multiplies the presented signal by zero (open) for all time exclusive of the interval $[0, T]$. Over $[0, T]$, the signal is multiplied by unity (closed). In a sampled system, the interval $[0,T]$ is replaced by N samples taken at a sample rate f_s where $T=N/f_s$. When the observation interval (i.e., N) becomes small, the quality of the spectral estimate begins to deteriorate. This consequence is called the *finite aperture effect.*

Windowing is a technique that tends to improve the quality of a spectrum obtained from a limited number of samples. Some of the more popular windows found in contemporary use are the rectangular or uniform window, the Hamming window, the Hann window, the Blackman window, and the Kaiser window.

Windows can be directly applied to FIRs. To window an N-point FIR, simply multiply the tap weight coefficients C_i with the corresponding window weights w_i. Note that all of the standard window functions have even symmetry about the midsample. As a result, the application of such a window will not disturb the linear phase behavior of the original FIR.

16.8.10 Multirate Signal Processing

Digital signal processing systems accept an input time series and produce an output time series. In between, a signal can be modified in terms of its time and/or frequency domain attributes. One of the important functions that a digital signal processing system can serve is that of sample rate conversion. As the name implies, a sample rate converter changes a system's sample rate from a value of f_{in} samples per second to a rate of f_{out} samples per second. Such devices are also called multirate systems since they are defined in terms of two or more sample rates. If $f_{in} > f_{out}$ then the system is said to perform decimation and is said to be decimated by an integer M if

$$M = \frac{f_{out}}{f_{in}} \tag{16.173}$$

In this case, the decimated time series $x_d[n] = x[Mn]$, or every Mth sample of the original time

ATTACHMENT II

4.16 Discrete-Time (Digital) Filters

Just as in the case of continuous-time (analog) filters, a discrete-time (digital) filter is a signal processor designed to allow signal components of certain frequencies to pass through to the output while preventing input signal components of other frequencies from doing so. The frequency response $H(e^{j\omega})$ should ideally have magnitude one in the passbands and magnitude zero in the stopbands.

Common Filter Types

The common types of discrete-time filters are the same as those for continuous-time filters, the only difference being that the frequency response $H(e^{j\omega})$ is completely specified by its values in the frequency range $0 \leq \omega \leq \pi$ as opposed to $0 \leq \omega < \infty$. The comments made regarding ideal and nonideal (practical) continuous-time filters apply directly to discrete-time filters as well.

Some significant differences with continuous-time filters exist regarding linear phase. Again, linear phase ensures that the shape of a signal is preserved in the filtering process. In discrete-time filters, however, true linear phase may in fact be achieved, but only if the filter is FIR. The FIR filter

$$H(z) = \sum_{r=0}^{M} b_r z^{-r}$$

will have linear phase if and only if

$$b_r = b_{M-r}, \qquad 0 \leq r \leq M,$$

i.e., if and only if the coefficients b_r are symmetric. It is important to point out that if M is odd then $H(z)$ will have a zero at $z = -1$, or equivalently $H(e^{j\omega})$ will be zero at $\omega = \pi$. This rules out the use of odd values of M in this situation if it is desired to construct a highpass or bandstop filter.

FIR Filter Design

Different techniques are employed for the design of FIR and IIR discrete-time filters, so these will be discussed separately. For simplicity, in the case of FIR filters, we will only consider linear phase filters with M even.

One method for designing FIR filters is known as windowing. This procedure begins by specifying the impulse response $h_i[n]$ of the desired ideal filter, assumed to have zero phase. Anticipating an even M, this quantity is given in Table 4.13 for the common filter types, with cutoff frequencies ω_c, ω_l, and ω_u.

A simple way to obtain an FIR filter from $h_i[n]$ is to truncate it at $n = \pm M$ and then shift the response to the right by $M/2$ to result in a causal linear phase FIR filter. However, since it is recalled that the $h_i[n]$ (actually $h_i[-n]$) are the Fourier series coefficients of $H(e^{j\omega})$ (with ω interpreted as the independent variable), this process amounts to Fourier series truncation, with its attendant Gibb's phenomenon oscillations.

Table 4.13 Common FIR Impulse Responses

Filter type	$h_i[0]$	$h_i[n],\ n \neq 0$
Lowpass	$\frac{\omega_c}{\pi}$	$\frac{\sin(n\omega_c)}{n\pi}$
Highpass	$1 - \frac{\omega_c}{\pi}$	$\frac{-\sin(n\omega_c)}{n\pi}$
Bandpass	$\frac{\omega_u - \omega_l}{\pi}$	$\frac{\sin(n\omega_u) - \sin(n\omega_l)}{n\pi}$
Bandstop	$1 - \frac{\omega_u - \omega_l}{\pi}$	$\frac{\sin(n\omega_l) - \sin(n\omega_u)}{n\pi}$

Table 4.14 Responses from Commonly Used Windows

Window	$w[n],\ 0 \leq n \leq M$[†]
Rectangular	1
Bartlett	$1 - \frac{2}{M}\left\lvert n - \frac{M}{2}\right\rvert$
Hanning	$\frac{1}{2} - \frac{1}{2}\cos\left(\frac{2\pi n}{M}\right)$
Hamming	$0.54 - 0.46\cos\left(\frac{2\pi n}{M}\right)$

[†] $w[n] = 0$ outside of this range.

Since these oscillations are normally unacceptable, a better approach is to reduce the effects of Gibb's phenomenon by multiplying the ideal impulse response by a tapered function known as a window, after first shifting the response to the right to produce causality. The impulse response $h[n]$ of the resulting filter is given by

$$h[n] = h_i[n - M/2]\,w[n], \qquad -\infty < n < \infty$$

where $w[n]$ is a symmetric window satisfying

$$w[n] = \begin{cases} w[M-n], & 0 \leq n \leq M \\ 0, & \text{otherwise} \end{cases}$$

The resulting filter is then

$$H(z) = \sum_{r=0}^{M} b_r z^{-r},$$

where

$$b_r = h[r], \qquad 0 \leq r \leq M.$$

Numerous choices for windows exist. Some commonly used windows are listed in Table 4.14 and shown in Figure 4.13.

It is noted that use of a rectangular window is equivalent to simply truncating the Fourier series. As we move down in the table, the windows are increasingly better at reducing the oscillations caused by Gibb's phenomenon. Generally, windows that

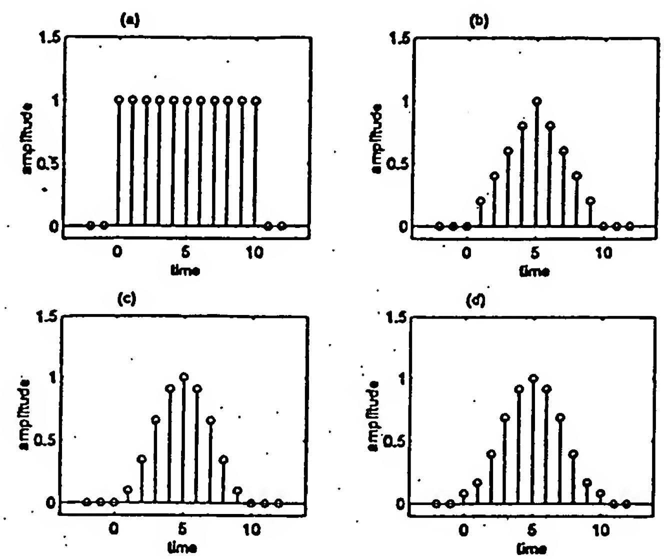

Figure 4.13 Four popular windows (shown for $M = 10$): (a) rectangular, (b) Bartlett, (c) Hanning, and (d) Hamming.

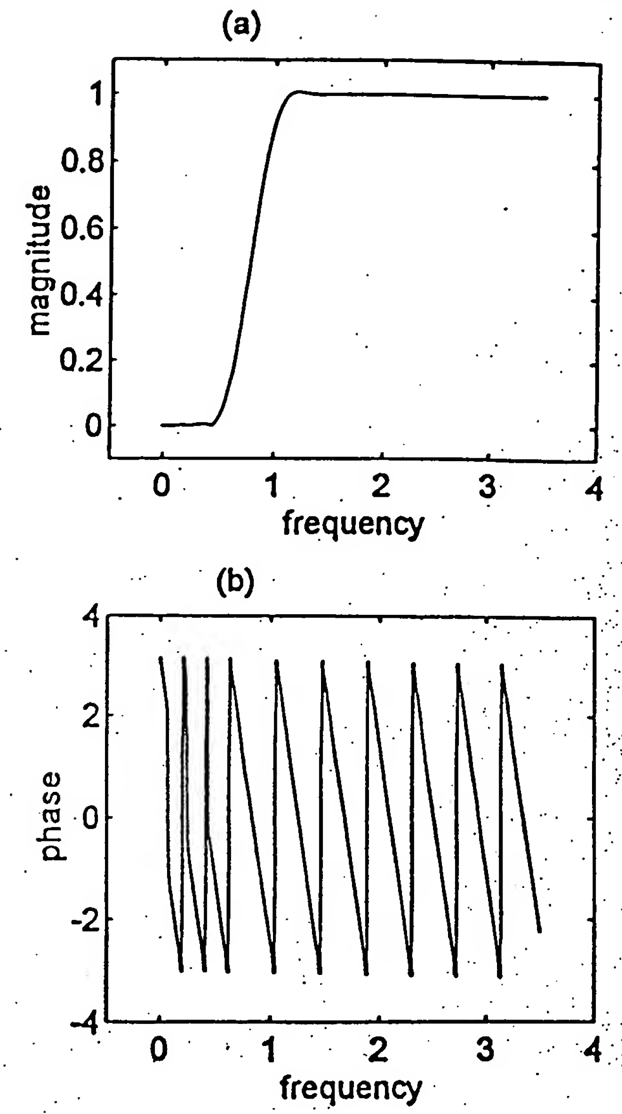

Figure 4.14 Highpass FIR linear phase filter (a) magnitude response and (b) phase response.

are good in reducing these oscillations do so at the expense of increased transition bandwidths.

As an example of using windowing to design a linear phase FIR filter, suppose we wish to construct a highpass filter with a cutoff frequency $\omega_c = \pi/4$ and a length $M = 30$. Choosing a Hanning window and following the procedure just discussed results in the filter

$$H(z) = \sum_{r=0}^{30} b_r z^{-r},$$

where

$$b_r = \frac{\sin\left((r-15)\dfrac{\pi}{4}\right)}{2(r-15)\pi}\left[\cos\left(\frac{\pi r}{15}\right) - 1\right],$$

$$r = 0, 1, \ldots, 30,\ r \neq 15,$$

and $b_{15} = 3/4$. Figure 4.14 illustrates the result of this design procedure.

While windowing has the advantage of being very simple, it has some significant drawbacks. These are the fact that there is no direct link with the tolerances specified by the designer and the fact that the tolerances in the various filter bands are not independently controllable.

A very popular method for FIR filter design, which does not suffer from these drawbacks, is the Parks-McClellan algorithm. Readily available and easy-to-use computer implementations of this algorithm exist. The Parks-McClellan algorithm results in FIR filters that are equiripple in all passbands and stopbands. The designer simply specifies the passband and stopband edges, the desired magnitude response in each band, the relative tolerances, and the filter order. The algorithm produces the resulting [illegible]

bands is not the concern of the algorithm, the magnitude response in these regions must be separately checked to ensure acceptability.

IIR Filter Design

The design of an IIR discrete-time filter usually involves the design of a continuous-time lowpass prototype filter, its transformation to a lowpass IIR discrete-time filter, and if necessary, a frequency transformation to produce the desired filter type. When simultaneously discussing continuous-time and discrete-time quantities, we will use Ω to represent continuous-time angular frequency while retaining ω for discrete-time angular frequency.

The design process begins by establishing the discrete-time filter specifications in precisely the same manner as in the case